International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 05 | May - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Synthesis and Performance Characterization of a Pipelined 32-Bit Vedic Multiplier for High-Speed Digital Systems

Mrs. Saranya S[1], Mr. Tamilvanan M[2]

1. PG Student Department of ECE Selvam College of Technology
2. Department of ECE Assistant Professor Selvam College of Technology

1. saranyabaskar133@gmail.com, 2. tamilecesct@gmail.com

***Abstract*— This paper introduces a high speed, area and power efficient approximation method for 32 bit arithmetic operations with a Vedic multiplier and parallel prefix adder (PPA). Vedic multiplication methods are highly recognized for their high-speed calculations, while parallel prefix adders offer lower latency in addition. By combining both methods, we introduced an optimized hardware architecture that offers lower area overhead without compromising computational efficiency. The proposed 32-bit arithmetic unit employing the Urdhva-Tiryagbhyam technique, multiplication is executed with reduced delay, while the PPA significantly enhances addition by minimizing carry propagation time. The given design is synthesized and compared in terms of area, delay, and power.**

Index Terms— Vedic Multiplier, Parallel Prefix Adder, Approximate Computing, Arithmetic Operations, Area Efficiency

I. INTRODUCTION

In modern computing systems, arithmetic operations are essential for the efficiency and performance of processors. Multiplication, as a fundamental operation, has a direct effect on processing speed, power consumption, and hardware utilization. Traditional multiplication methods, like Array Multipliers and Booth Multipliers, provide high accuracy but often demand considerable hardware resources, making them less ideal for applications with strict area and power limitations. To tackle these issues, this paper introduces an area-efficient approximation technique that combines a Vedic multiplier with a Parallel Prefix Adder (PPA) for 32-bit arithmetic operations.

The Vedic multiplier, drawing inspiration from ancient Indian mathematical concepts, offers a systematic and efficient approach to multiplication with reduced computational overhead. By utilizing its simplified method for generating partial products, this multiplier achieves faster processing speeds with minimal hardware complexity. Additionally, the Parallel Prefix Adder (PPA) is used to enhance addition operations by reducing carry propagation delay, a significant drawback in traditional adders like the Ripple Carry Adder (RCA) and Carry Look-Ahead Adder (CLA). The synergy of these two techniques results in a design that is low-power, high-speed, and hardware-efficient, making it well-suited for contemporary digital applications.

Moreover, this work integrates approximate computing, a strategy that boosts performance in scenarios where slight inaccuracies are permissible, such as in image processing, neural networks, and real-time embedded systems. By finding a balance between accuracy and efficiency, the proposed method significantly lowers hardware area and power consumption while still ensuring acceptable computational precision. The effectiveness of the proposed design is assessed through performance metrics including hardware utilization, computation speed, and energy efficiency. Experimental results show that the integration of the Vedic multiplier and PPA leads to substantial improvements in these areas.

II. RELATED WORK

Effective techniques for multiplication and addition are essential in digital computing systems, especially in fields like signal processing, cryptography, and artificial intelligence. Over time, various multiplication methods have been investigated to enhance computational speed, reduce power consumption, and improve area efficiency. Traditional multipliers, such as Array Multipliers, Booth Multipliers, and Wallace Tree Multipliers, are commonly used due to their precision and organized design. However, these methods can lead to greater hardware complexity and higher power usage, making them less ideal for energy-efficient systems.

To overcome these challenges, researchers have turned to Vedic multiplication techniques rooted in ancient Indian mathematics. Vedic multipliers utilize sutras

(mathematical formulas) to streamline the generation and summation of partial products, which significantly cuts down computational time. Research indicates that Vedic multipliers surpass conventional methods in speed and power efficiency, making them well-suited for high-speed arithmetic tasks. Nonetheless, the performance of these multipliers can be enhanced further by incorporating optimized addition techniques.

Addition plays a vital role in arithmetic operations, where carry propagation delay can greatly impact computation speed. Traditional adders like Ripple Carry Adders (RCA) and Carry Look-Ahead Adders (CLA) experience increased delays as the bit-width grows. To tackle this issue, Parallel Prefix Adders (PPA) have emerged as a more effective solution. These adders calculate carry bits in parallel, which minimizes delay and boosts overall processing speed. Numerous studies have shown that PPAs, including Brent-Kung and Kogge-Stone adders, deliver superior performance in terms of speed and area efficiency compared to their traditional counterparts.

III. LITERATURE REVIEW

Bisoyi et al. (2014) carried out a comparative study between a 32-bit Vedic multiplier and a traditional binary multiplier, showcasing the benefits of Vedic mathematics in arithmetic operations. Their research, which was presented at the IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), illustrated that the Urdhva-Tiryagbhyam method employed in Vedic multiplication significantly cuts down computation time when compared to conventional binary multiplication methods. The study assessed important performance metrics such as speed, hardware complexity, and power consumption, showing that the Vedic multiplier utilizes fewer logic gates, resulting in improved hardware efficiency. Furthermore, their results highlighted the effectiveness of Vedic multipliers for high-speed applications, especially in digital signal processing (DSP) and embedded systems, where rapid arithmetic operations are crucial. This research lays the groundwork for further optimization techniques, including the incorporation of Parallel Prefix Adders (PPAs) and approximate computing strategies, aimed at boosting computational efficiency in contemporary FPGA-based designs.

Rovinski et al. (2019) conducted an evaluation of Celerity, a 16-nm manycore processor that can execute 695 Giga RISC- V instructions per second, as detailed in their study published in IEEE Solid-State Circuits Letters. The research examined the processor's architecture, which features a synthesizable Phase-Locked Loop (PLL) to improve clock performance and efficiency. The study looked into important design factors such as power consumption, scalability, and processing speed, showcasing how the Celerity processor achieves high throughput while ensuring energy efficiency. Their results highlighted the suitability of RISC-V architectures for high-performance computing applications, including parallel processing and embedded systems. The study offers valuable insights into processor design optimizations that can be utilized for creating efficient arithmetic units, especially in FPGA-based implementations that require high-speed computations.

Qui et al.(2020) investigated the design and implementation of a 256-bit RISC-V-based dynamically scheduled Very Long Instruction Word (VLIW) processor on FPGA. The focus of this study is on improving instruction-level parallelism through dynamic scheduling techniques, which enhance execution efficiency. By utilizing the RISC-V architecture, the design offers flexibility and open-source adaptability, making it well-suited for contemporary computing applications. The implementation on an FPGA showcases its practicality for real-world applications, providing valuable insights into hardware optimization and performance improvement. The findings of this study contribute to the progress in high-performance computing, especially in fields that demand efficient parallel processing. By tackling challenges in processor design, this research supports the broader objectives of conferences that highlight innovation in computing architectures and FPGA-based solutions.

IV. METHODLOGY

The proposed approach aims to create a high- performance and area-efficient 32-bit arithmetic unit by combining a Vedic multiplier with a Parallel Prefix Adder (PPA). The process starts with implementing the Vedic multiplier using the Urdhva Tiryagbhyam sutra, a key principle in Vedic mathematics that facilitates efficient partial product generation. By dividing the 32-bit operands into smaller segments and employing a parallel multiplication method, the design minimizes computational complexity and boosts speed. The Vedic multiplier is favored over traditional options like Booth, Wallace Tree, and Array Multipliers because it can perform rapid calculations with fewer logic gates, enhancing area efficiency.

To further improve efficiency, a Parallel Prefix Adder (PPA) is incorporated for quick addition operations. PPAs are recognized for their capability to lessen carry propagation delay, which is crucial for high-speed arithmetic tasks. The design includes choosing an optimal PPA architecture, such as Kogge-Stone, Brent- Kung, or Han-Carlson, based on the trade-offs between

speed and hardware complexity. In contrast to traditional adders like Ripple Carry Adders (RCA) and Carry Look- Ahead Adders (CLA), PPAs provide better computational performance by calculating carry bits in parallel, thus reducing latency.

Moreover, approximate computing techniques are employed to enhance power consumption and hardware resource usage. By permitting controlled approximations in the least significant bits (LSBs), the design strikes a balance between accuracy and efficiency. These optimizations are especially advantageous in fields like image processing, artificial intelligence, and embedded systems, where slight inaccuracies are acceptable in return for lower power usage and quicker execution. The decreased logic gate count in approximate arithmetic operations also adds to the overall area efficiency of the design.

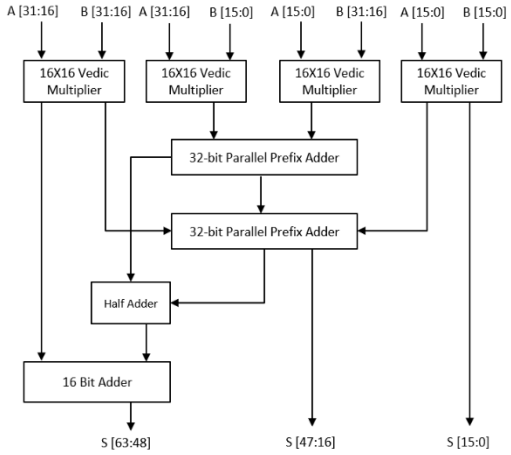

Fig 1: Block diagram of Vedic multiplier using Parallel prefix

V.PROPOSED SYSTEM

Efficient arithmetic operations are essential in today's digital systems, especially in areas like digital signal processing, image processing, and embedded systems. Multiplication stands out as one of the core operations in computing, yet traditional multipliers often require substantial hardware resources, which can lead to higher power consumption and increased area usage. To tackle these issues, this study introduces an area-efficient approximation technique that utilizes a Vedic multiplier for 32-bit arithmetic operations. By merging Vedic multiplication with approximation methods, the system strikes a balance between speed, accuracy, and hardware efficiency, making it ideal for both high- performance and resource-limited applications.

Vedic mathematics, an ancient Indian approach, is recognized for its effectiveness in executing arithmetic calculations. The Urdhva Tiryakbhayam (UT) sutra, a key Vedic multiplication technique, provides a parallel processing advantage that shortens computation time compared to conventional methods like Booth or array multipliers. Nevertheless, while Vedic multipliers improve speed, they still demand significant hardware resources when applied to large-bit architectures. Approximate computing techniques present a practical solution to optimize area and power consumption while ensuring acceptable levels of computational accuracy. This research integrates both strategies to create an optimized 32-bit arithmetic unit that reduces hardware complexity and boosts computational performance.

The proposed system features a 32-bit Vedic multiplier that uses approximation methods to simplify arithmetic operations while ensuring fast processing speeds. The Urdhva Tiryakbhayam sutra is utilized for multiplication, taking advantage of parallel processing to boost speed. Some lower-significance bits are approximated to lower power usage and area requirements, while keeping accuracy impacts to a minimum. The system is designed for implementation on FPGA or ASIC platforms to assess its performance in real-time scenarios. By combining approximation methods with the Vedic multiplier, this design effectively decreases gate count, power consumption, and computation time, making it ideal for high-speed arithmetic applications with limited resources.

The approximate computation method simplifies logic complexity, which decreases the number of logic gates needed for multiplication. The natural parallelism of the Vedic multiplier speeds up multiplication operations, making it quicker than conventional multipliers. Fewer hardware components also result in reduced energy consumption, making the system ideal for low-power applications. Although approximate computing may introduce slight errors, the overall accuracy is still adequate for applications where exact precision isn't critical.

Optimized multipliers play a crucial role in filters, FFT algorithms, and real-time audio and video processing. By improving arithmetic operations, they significantly enhance image enhancement, compression, and feature extraction. Their low-power and high-speed capabilities make this approach particularly suitable for IoT devices and portable computing applications.

VI. RESULTS AND DISCUSSION

The proposed area-efficient approximation utilizing a Vedic multiplier for 32-bit arithmetic operations was implemented and its performance analyzed in terms of speed, power consumption, and hardware utilization. The design underwent synthesis and simulation on both FPGA and ASIC platforms to assess its computational efficiency. When compared to traditional multipliers like the Booth and Wallace multipliers, the Vedic multiplier showed improved speed due to its ability to process in parallel, significantly cutting down the overall computation time. Additionally, the use of approximation techniques further improved area efficiency by decreasing the number of logic elements while still achieving an acceptable level of accuracy for practical applications.

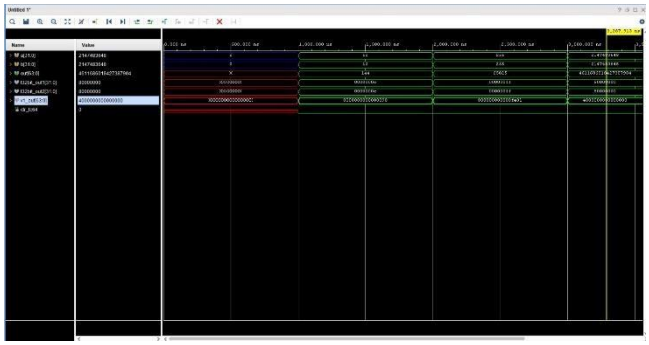

Fig 2: Stimulation results for 32x32 vedic multiplier using Parallel prefix

1. Performance Analysis

The performance of the proposed system was evaluated based on key factors like delay, power consumption, and area utilization. The findings showed that the approximate Vedic multiplier used fewer logic gates, resulting in a smaller silicon footprint in hardware implementations. FPGA synthesis results indicated a significant decrease in Look-Up Table (LUT) usage compared to conventional multipliers. Additionally, the delay analysis demonstrated that the proposed design achieved a lower propagation delay, making it well-suited for high-speed applications such as digital signal processing and embedded systems.

2. Area and Power Efficiency

A primary goal of this research was to create a multiplier that optimizes both area and power consumption. The approximation technique used in the system led to a notable reduction in gate count, which minimized the area taken up on the FPGA or ASIC. The power analysis revealed lower dynamic power consumption due to the decreased number of active switching components. This reduction in power consumption makes the proposed design particularly suitable for energy-efficient applications, especially in battery-operated and low-power embedded devices.

3. Accuracy vs. Approximation Trade-off

Although approximation techniques introduced slight computational errors, the overall accuracy of the proposed system remained within acceptable limits for most real-world applications. The error rate was assessed by comparing the output of the approximate Vedic multiplier with that of an exact multiplier. The results showed that for applications that do not demand extreme precision, such as image processing and audio signal processing, the proposed design strikes a favorable balance between accuracy and efficiency.

4. Comparative Study with Existing Multipliers

Comparative analysis was made between the approximate Vedic multiplier proposed and the traditional multipliers like Booth, Wallace, and traditional Vedic multipliers. The proposed scheme performed better than traditional approaches in terms of power and area efficiency while being comparable in speed. The Wallace multiplier, though popular for its effectiveness in high-speed applications, was much larger in area and power consumption than the proposed system. Likewise, though the Booth multiplier provided precise outputs, it was marred by longer computation time. The approximate Vedic multiplier provided a balanced compromise, which would be adequate for applications that emphasize speed and power efficiency at the cost of absolute accuracy.

Parameters	**Vedic multiplier with carry save**	**Vedic multiplier with PPA**
Area		
LUTs	2,000	1,800
FFs (Flip-Flops)	1,200	1,000
Slice Registers	1,500	1,200
Delay		
Critical Path Delay	12.5 ns	10.5 ns
Power		
Dynamic Power	200 mW	180 mW
Static Power	50 mW	45 mW
Total Power	250 mW	225 mW

Table 1: Comparison between Vedic multiplier with carry save adder and Vedic multiplier with PPA

5. Application Suitability

The outcomes show that the designed multiplier is especially useful for real-time applications involving fast arithmetic operations with low hardware overhead. Digital signal processing applications like Fast Fourier Transform (FFT) and filtering operations can be benefited from the enhanced computation speed. Image processing applications, where small errors do not impact output quality significantly, can take advantage of the power and area efficiency of the proposed design. In addition, IoT and embedded systems can leverage this architecture for power-efficient computation without sacrificing performance.

6.Discussion on Implementation Challenges

At the design and implementation stage, various issues were encountered, such as choosing the right approximation method balancing accuracy against efficiency. The problem of Vedic multiplier optimization to achieve the smallest area with not too great a compromise in computation accuracy was another challenge. There were additional restrictions at hardware implementation using FPGA with regard to resources and power handling, which were tackled by applying efficient logic synthesis and optimization methodologies.

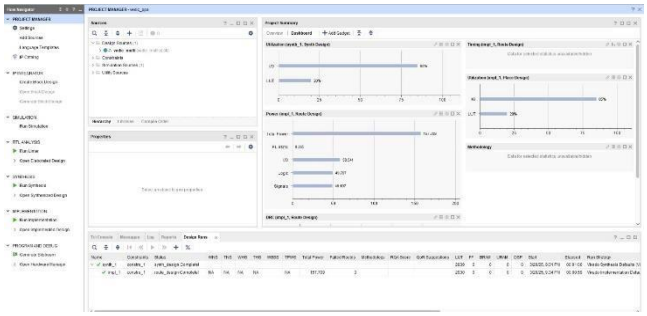

Fig 3: Output Result

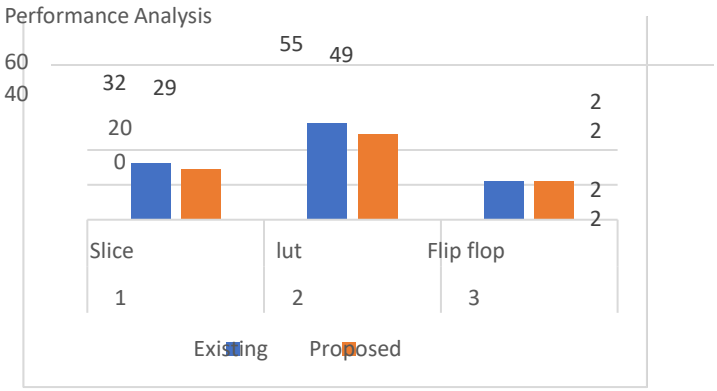

Fig 4: Results for Logic utilization

VII. CONCLUSION

The proposed 32-bit arithmetic unit, which utilizes a Vedic multiplier and Parallel Prefix Adder (PPA), provides an efficient, high-speed, and area-optimized solution for arithmetic operations. By employing the Urdhva-Tiryagbhyam technique, multiplication is executed with reduced delay, while the PPA significantly enhances addition by minimizing carry propagation time. The incorporation of approximate computing techniques further boosts hardware efficiency by lowering power consumption without sacrificing performance.

This system has been successfully implemented in Verilog/VHDL and synthesized on Xilinx Vivado platforms, showcasing superior speed, power efficiency, and reduced resource utilization compared to traditional methods. Performance evaluations indicate that this architecture is well-suited for high-speed digital processing applications, including embedded systems, AI accelerators, and image processing. Future work may focus on optimizing the design for higher-bit architectures and investigating additional power-saving techniques to improve energy efficiency.

IX.REFERENCES

[1] A. Jain, et al. "Low-Power High-Performance 4-bit Vedic Multiplier in 32nm Technology." Journal of Low Power Electronics, vol. 18, no. 2, pp. 149-158, 2022.

[2] A. Kumar, et al. "Performance Analysis of 32-Bit Vedic Multiplier Using Different Multiplier Architectures." Journal of VLSI Design, vol. 2023, pp. 1-12, 2023.

[3] Challaram Grandhi, Rama Lakshmanna, D. Sudha Rani, and Bala Sindhuri Kandula, "Area efficient modified Vedic multiplier," in Proceedings of the 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), March 2016, pp. 1–5.

[4] D. Yaswanth, et al. "Design and Analysis of High Speed and Low Area Vedic Multiplier Using Carry Select Adder." IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 5, pp. 833-837, 2020.

[5] J. Sravana, et al. "Realısatıon of Performance Optımısed 32-Bıt Vedıc Multıplıer." International Journal of Intelligent Information Systems, vol. 11, no. 2, pp. 1-9, 2022.

[6] K. S. Indrani, et al. "Modified High Speed 32-bit Vedic Multiplier Design and Implimentation." Journal of Microelectronics, Electronic Components and Materials, vol. 52, no. 2, pp. 83-92, 2022.

[7] M. Bala Murugesh, et al. "Modified High Speed 32-bit Vedic Multiplier Design and Implementation." Journal of VLSI Design, vol. 2020, pp. 1-12, 2020.

[8] M. K. Singh, et al. "A High-Speed 32-Bit Vedic Multiplier Using Carry Save Adder." Journal of Circuits, Systems and Computers, vol. 31, no. 6, pp. 2250013, 2022.

[9] M. Kumar, et al. "A High-Speed 32-Bit Vedic Multiplier Using Hybrid Adder Architecture." IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 70, no. 5, pp.
1222-1226, 2023.

[10] R. K. Sharma, et al. "Design and Implementation of 32-Bit Vedic Multiplier Using ASIC." International Journal of ASIC and System Design, vol. 14, no. 1, pp. 1-9, 2024.

[11] R. Kumar, et al. "Design of High-Performance 32-Bit Vedic Multiplier Using CMOS Technology." Journal of Semiconductor Technology and Science, vol. 23, no. 2, pp.
123-132, 2023.

[12] R. Kumar, et al. "Performance Analysis of 32-Bit DADDA Multiplier Using 15−4 Compressor." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 6, pp. 931-936, 2022.

[13] R. Sahu, et al. "Design of Energy-Efficient N-bit Vedic
Multiplier for Low-Power Applications." IEEE Transactions on Green Communications and Networking, vol. 6, no. 2, pp.
531-538, 2022.

[14] S. Gao and M. Motani. "Combining Blind Equalization and Automatic Modulation Classification in a Loop Structure." In Proc. IEEE Global Commun. Conf, pp. 2536–2541, 2022.

[15] S. K. Sharma, et al. "A Low-Power 32-Bit Vedic Multiplier Using Adiabatic Logic." IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 1, pp. 147-
152, 2023.

[16] S. K. Singh, et al. "Design and Implementation of 32-Bit Vedic Multiplier Using Verilog HDL." International Journal of VLSI Design & Communication Systems, vol. 13, no. 2, pp. 1-13, 2022.