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# Ultra-Low Power, Area Optimized CMOS Successive Approximation Based ADC for Mixed-Signal Systems

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**Abstract -** Analog signals are present everywhere in the form of sound or sensor readings. But today's digital systems, like microcontrollers and processors, can only work with binary numbers. For this we use analog-to-digital converters. Among the various ADC architectures, Successive Approximation Register (SAR) ADCs are widely preferred due to their low power consumption, small area, and moderate speed. However, existing SAR ADC designs still face major challenges such as high-power consumption, layout capacitor mismatch, and the requirement for stable reference voltages. These problems limit their accuracy, efficiency, and practical use in advanced applications. This Paper resolve these issues by designing four key blocks of a SAR ADC: a sample-and-hold circuit, comparator, SAR logic, and reference DAC. This Paper goal was to make the layout smaller and reduce power usage, while still ensuring accurate conversion.

***Key Words***: SAR Logic, Comparator, DAC, Low Power , Mixed Signal Systems

## 1.INTRODUCTION

Today's smartphones, medical wearables, and IoT sensors all rely on processing real world signals, whether sound, temperature, or body signals. These signals are mechanical signals, but digital systems cannot understand mechanical data. Analog-to-Digital Converters make sure the signals are converted to digital so they can be interpreted and processed in the computer. We have Flash ADCs, Pipeline ADCs, Sigma Delta ADCs, Successive Approximation Register (SAR) ADCs, and many more types of ADCs. Each type has its own advantages and drawbacks. Flash analog-to-digital converters offer very fast performance but at a high cost. Pipeline ADCs are also fast but need complex calibration. Sigma-Delta ADCs provide high accuracy but work slowly. Successive approximation register (SAR) converters act as an important link between real-world analog signals and the digital processing domain. They are often chosen in practical designs because they can achieve useful levels of resolution while keeping energy demands low, which makes them suitable for portable and low-power systems. As a result, they are the best choice for low-power medium speed applications. In recent years, there are many advancements in SAR ADC design. Researchers focused on eliminating power consumption, saving silicon area, increasing precision, etc. Early techniques like monotonic switching, merged capacitor switching, and VCM-based steering helped to reduce power consumption effectively. Recently, SAR ADC performance has improved due to hybrid switching methods, calibration circuits, and smaller CMOS technologies. Due to these attributes, SAR ADCs have become popular in portable electronics, IoT, biotech implants, and industrial automation. Flash ADC - not used because of high power area need Pipeline ADC - Stable but less dominant in low-power systems. Sigma-Delta ADC - Still used for high-precision, but niche SAR ADC - Rapidly growing from and becoming the most dominant ADC type due to low power, compact area, and good resolution. Even with their designing SAR ADCs is not straightforward. The main elements—such as the comparator, DAC, sample-and-hold unit, and control logic— interact in complex ways. Each block adds its own limitations, and achieving the desired overall performance requires carefully balancing these constraints. This paper provides a review of ADC architectures with a special focus on SAR ADCs, summarizing key advancements, identifying existing challenges, and highlighting future research directions to achieve ultralow-power and area optimized CMOS SAR based ADC for mixed signal system.

## 2. Overview

The design of ADC is important for mixed-signal system performances. Mixed-signal systems typically consist of analog interfaces and a digital processing unit on a single chip. The increasing craze of wearables, IoT nodes, biomedical implants, portable communication systems has created the need for converters that consume ultra-low power, occupy tiny silicon area but still provide decent resolution and speed. The best architecture that has come up in this case is the SAR ADC A SAR ADC requires only one comparator and a capacitor based DAC. This makes SAR ADCs more energy efficient than Flash and Pipeline

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architectures. The conversion process uses a binary search algorithm. In this algorithm, the input signal is sampled. After that, it is compared to a number of reference voltages. The reference voltages are generated by DAC. This step-by-step approximation removes the need for large arrays of comparators or complex multi-stage pipelines, which greatly reduces power and chip area. The digital SAR logic can scale with CMOS technology, making the architecture suitable for future technology nodes. A lot of effort is being put towards improving the DAC switching mechanism for ultra-low power. Traditional switching techniques require substantial energy because of frequent charging redistribution in the capacitor array. Designing a high-performance class d power amplifier using an enhanced modulator for accurate pulse-width modulation. With these methods energy reductions can be as much as 90% compared to the conventional one which helps in achieving femtojoule-per-conversion-step in a SAR. In addition, dynamic comparators are employed, which only consume current during the comparison phase, further reducing static power consumption. Another important consideration for mixed-signal systems is area optimization SAR ADC design. The capacitor DAC takes up most of the ADC area, especially in high resolution designs. Techniques like segmented capacitor arrays, capacitor scaling, and layout-aware matching have been introduced by researchers to reduce silicon area without compromising on accuracy. However, these methods come with challenges of capacitor mismatch and parasitic effects, which can hurt linearity. To avoid this complication, most recent SAR ADCs now use background calibration, which can automatically correct for any mismatch and comparator offset during normal operation. Ultra-low power area efficient SAR ADCs have a lot of applications. ADC for implantable and wearable sensors in biomedical systems, for example, should consume as little energy as possible to prolong battery life, or enable energy harvesting. IoT devices use SAR ADCs to access data from physical sensors. Energy efficiency determines how long the system will last. In communication systems, SAR ADCs are integrated analog-to-digital converters which act as front ends to any communication circuit. Despite these advances, several challenges remain. It remains challenging to keep linearity and high ENOB while continuously shrinking the size of the capacitor. Moreover, achieving a sub-femtojoule energy per conversion-step across process, voltage, and temperature variations remains an open research problem. Moreover, design and calibration must consider the non idealities of the sample-and-hold circuit and the mismatch in the scaled CMOS processes. In conclusion, the ultra-low power and area-optimized SAR ADC stands out as the leading candidate for mixed-signal systems in advanced CMOS technology. Its balance of efficiency, compactness, and adaptability makes it highly suitable for emerging low power applications. Ongoing research continues to address the challenges of mismatch, noise, and scaling effects, with the ultimate goal of delivering converters that achieve robust, sub-femtojoule energy performance in real silicon implementations.

## 3. Problem Statement

The advanced mixed-signal systems with portable devices need ADCs with low power and area. Among all architectures, it is the Successive Approximation Register ADC which has come out to be the most suitable because it offers a good tradeoff between resolution, power consumption and integration in CMOS technology. Challenges remain in designing SAR ADC in advanced technology nodes despite its advantages. The Sample-and Hold (S/H) circuit suffers from charge injection, clock feedthrough, leakage, and thermal noise that degrade accuracy and reduce effective resolution. Furthermore, the capacitor-based DAC, which is the biggest contributor of power and silicon area to the ADC, suffers from mismatch and parasitic effects at deep-submicron nodes causing large non-linearity errors. Researchers have come up with energy efficient switching scheme and calibration scheme to tackle these issues; however, most of the solutions either make the circuit complex, require more area or do not remain robust over PVT. Therefore, the main problem tackled in this work is the design and optimization of a Sample-and-Hold circuit and DAC of a SAR ADC implemented in CMOS. The aim is to achieve low power and small silicon area while accepting resolution and accuracy and hence making the design suitable for modern mixed-signal.

## 4. Proposed Work

The project Ultra-low power, area optimized CMOS Successive approximation based ADC for mixed signal systems , designing in MICROWIND and DSCH Software. The block diagram is as follows:These mainly consist four blocks for designing purpose that is Sample and Hold Circuit which is basically frontend of This Paper. Then comparator comes in picture which convert analog signal to digital signal and another one is successive approximation register and Digital to analog converter.

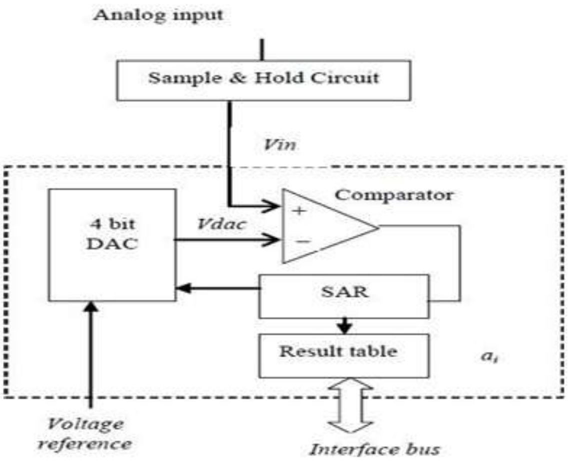

Fig : SAR ADC Block Diagram

**Sample And Hold Circuit** : Sample and hold circuit is frontend of a circuit. It is an important block in an ADC that captures the instant value of an analog input signal during the sampling phase and holds it steady during the conversion phase. One of the most efficient and widely used implementations of the S/H circuit is based on a transmission gate switch combined with a CMOS.

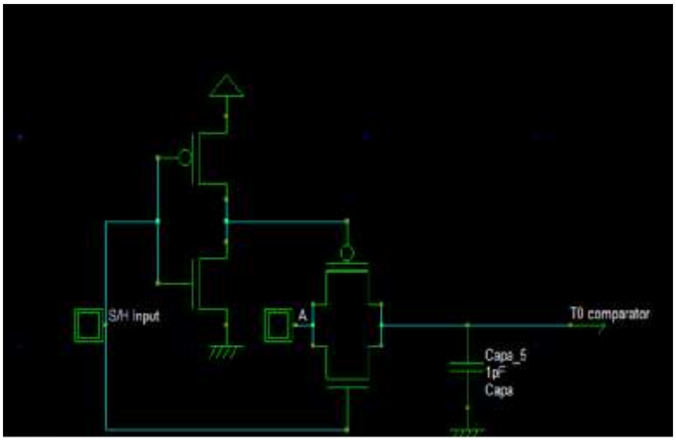

Fig : Transmission based Sample and hold circuit .SCH file

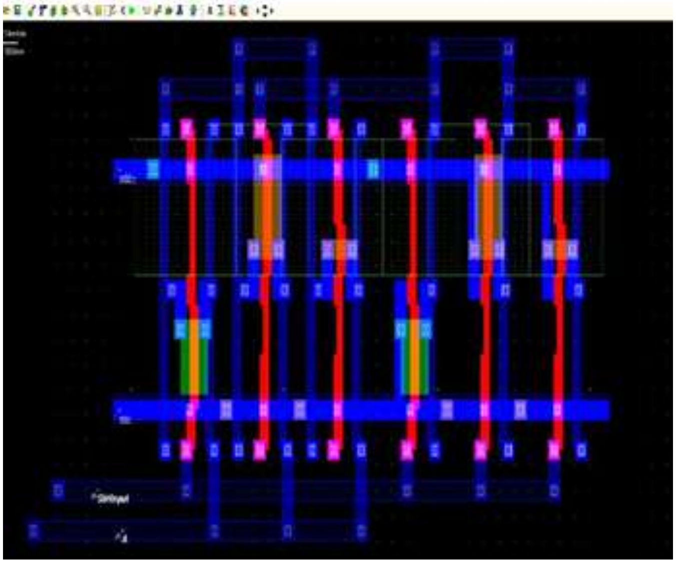

Fig: Compiled in Microwind

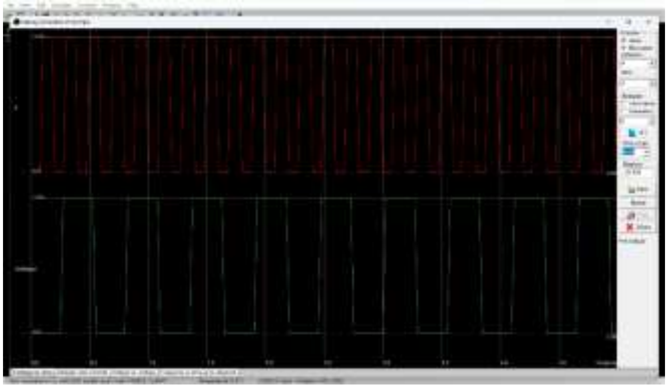

Fig : Output Waveform Of S/H Circuit

### A) Digital to analog converter

The Digital-to-Analog Converter (DAC) is an important block of the SAR ADC that converts the digital output generated by the SAR logic into an equivalent analog voltage. In the proposed design, an R–2R ladder DAC architecture is implemented due to its simplicity, accuracy, and reduced requirement of precise resistor values.

The implemented DAC consists of: Resistor ladder network using R = 10 kΩ and 2R = 20 kΩ, MOS switches controlled by SAR logic outputs, Reference voltage input, Analog output node connected to the comparator.

During operation, the SAR logic sequentially updates the digital bits, which control the switches of the R–2R ladder. The resulting analog voltage is generated at the output node and fed back to the comparator for further comparison with the sampled input voltage.

The use of only two resistor values simplifies fabrication and improves the reliability of the DAC implementation in CMOS technology.

Following figure shows the Schematic diagram, Dsch file, Microwind layout and implementation of Digital to analog converter (R-2R ladder):

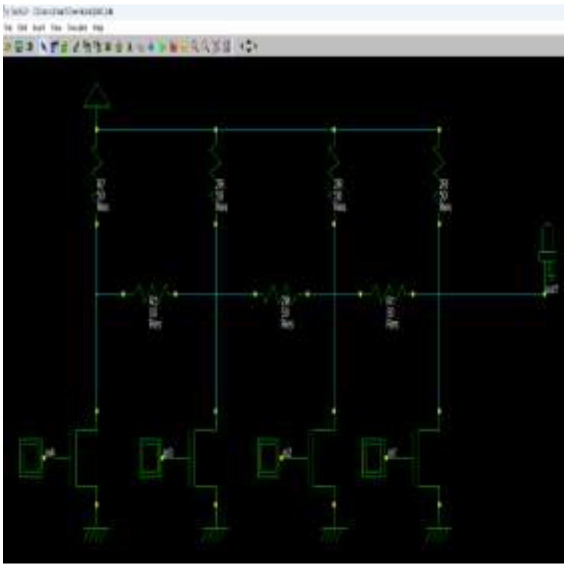

Fig 3.2: 4 bit R2R DAC .SCH file

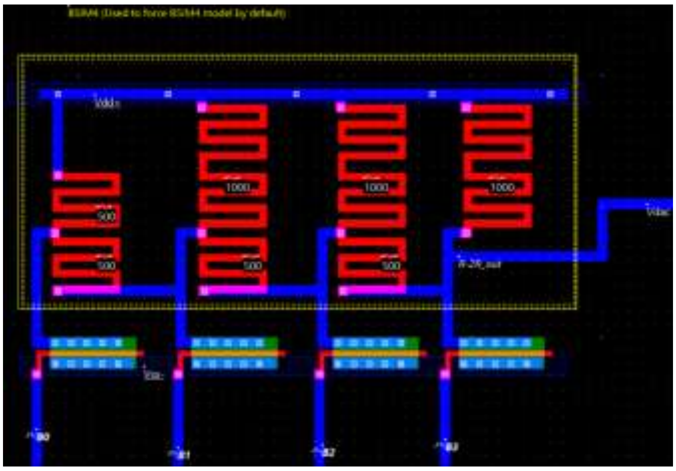

Fig: 4 bit R2R DAC . MSK file

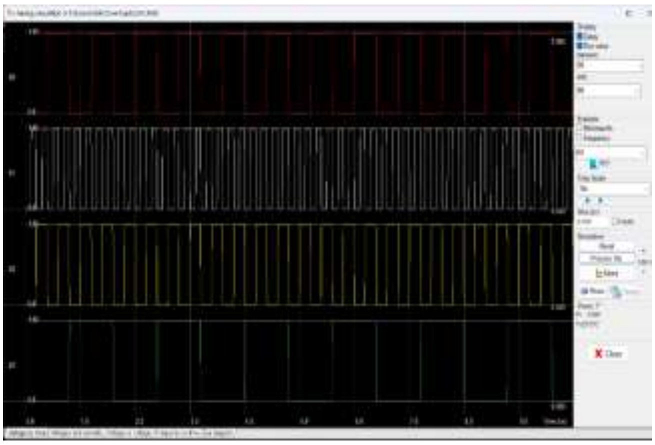

Fig: Output Waveform Of 4 bit R2R Circuit

### B) Dynamic latch Comparator

The comparator is a critical component of the SAR ADC as it determines whether the sampled input voltage is greater or smaller than the DAC output voltage.

The comparator performs the decision operation. If the input voltage is greater than the DAC output voltage, the comparator produces a logic high output, otherwise, it produces a logic low output.

The dynamic latch comparator operates in two phases controlled by the clock signal:

a) Reset Phase: During the reset phase, the clock signal is low, and the output nodes of the comparator are pre-charged to the supply voltage. The internal nodes are equalized to remove any previous comparison information and prepare the circuit for the next evaluation cycle.

b) Evaluation Phase: When the clock signal transitions to high, the comparator enters the evaluation phase. The differential input pair senses the voltage difference between the sampled input voltage and the DAC output voltage. This small voltage difference is amplified through positive feedback provided by the cross-coupled latch structure, resulting in a rapid transition of the output nodes to either logic high or logic low.

The use of a dynamic latch structure eliminates static power dissipation since current flows only during the evaluation phase. This makes the comparator highly suitable for low-power SAR ADC applications.

Following figure shows the Dsch file, Microwind layout and implementation of Dynamic Latch Comparator:

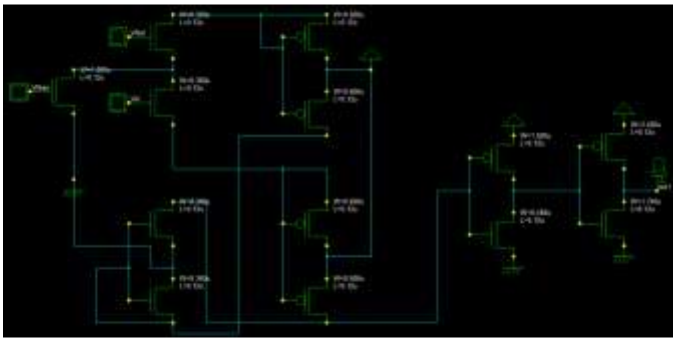

Fig: Dynamic Latch Comparator .SCH file

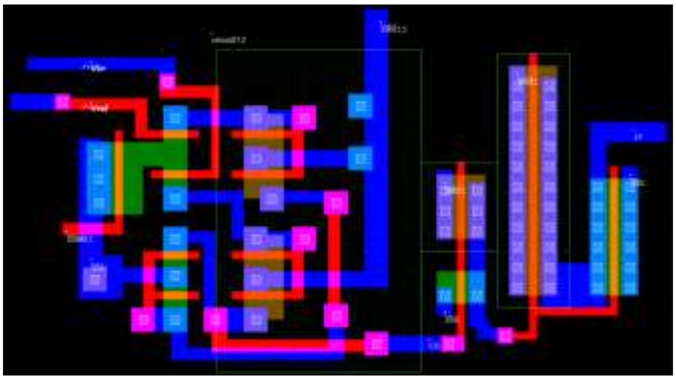

Fig:Dynamic Latch Comparator .MSK file

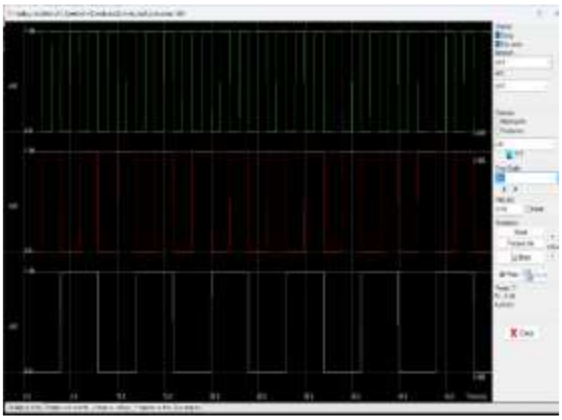

Fig 4.3: Output waveform of Dynamic Latch Comparator

### C) Successive Approximation Register (SAR) Logic

The Successive Approximation Register (SAR) logic controls the overall conversion process of the SAR ADC. It performs a binary search algorithm to determine the digital representation of the sampled analog input voltage. The SAR logic sequentially generates digital bits from the Most Significant Bit (MSB) to the Least Significant Bit (LSB) by interacting with the comparator and DAC blocks.During the conversion process, the SAR logic initially sets the MSB to logic ‘1’ while all other bits are cleared. The DAC converts this digital code into an analog voltage, which is then compared with the sampled input voltage using the dynamic latch comparator. Based on the comparator output, the SAR logic either retains the current bit value or resets it to logic ‘0’. This process continues sequentially for each bit until the complete digital code is obtained.

The operation of the SAR logic can be summarized as follows: The sampled input voltage is held by the Sample and Hold circuit, SAR logic sets the MSB to ‘1’, DAC generates the corresponding analog voltage, dynamic latch comparator compares the input voltage with the DAC output and If $V_{in} > V_{DAC}$, the bit remains ‘1’; otherwise it is reset to ‘0’. The SAR logic shifts to the next bit and repeats the comparison process and after all bits are evaluated, the final digital output code is produced.

The SAR logic circuit is implemented using digital components including D Flip-Flops, Shift registers, Logic gates, Clock control circuitry.

The digital schematic was designed and verified using DSCH 3.9, where timing simulations were performed to ensure correct sequential operation. After verification, the circuit was exported to Microwind 3.9 for transistor-level implementation and layout generation.

The SAR logic operates synchronously with the clock signal to control the sampling, comparison, and bit decision processes. Proper timing coordination between the SAR logic, DAC, and dynamic latch comparator ensures accurate and efficient analog-to-digital conversion.

The layout of the SAR logic block was optimized to minimize routing complexity and reduce propagation delay. Simulation results confirm that the SAR logic successfully performs the successive approximation algorithm and generates the correct digital output corresponding to the input analog signal.

Following figure shows the Dsch file, Microwind layout and implementation of Successive Approximation Register:

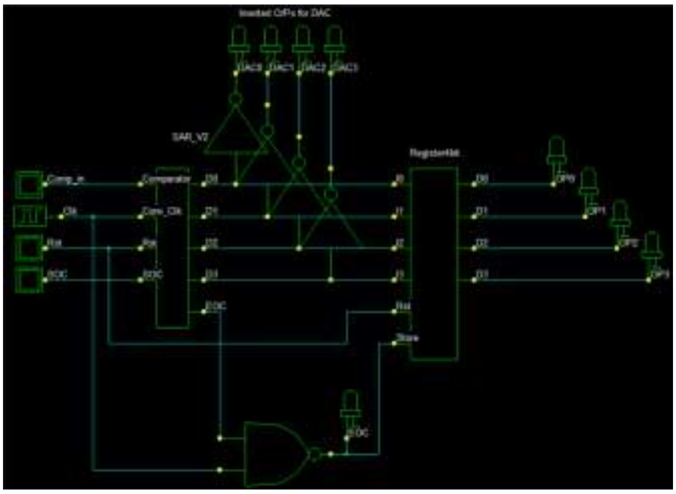

Fig : SAR Logic .SCH File

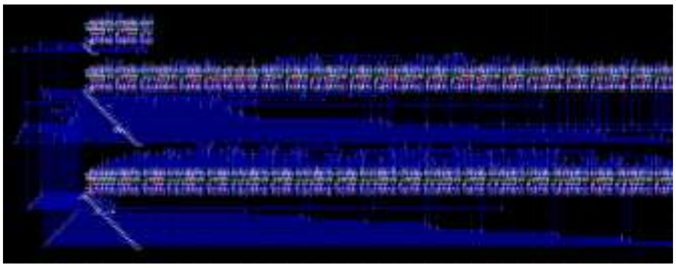

Fig : SAR Logic .Verilog File

### D) Pulse Generator

The SAR ADC operates smoothly with the help of the Pulse Generator that generates clock signals in sequential order to carry on the conversion process. The SAR ADC works in a successive manner in which each decision of the bit is achieved during a pulse of clock. As a result, there is a need for a stable and periodic pulse generator. It is needed to control the operation of the Sample and Hold circuit, the evaluation of the comparator, and the logic operation of the SAR.

A pulse generator creates a series of digital pulses that act as a timing reference for the system. The SAR ADC receives pulses to make sure that every block does its task at the right time intervals. Through use of digital logic circuits the digital level implementation of the pulse generator is done and the transistor level implementation is verified.

While operation, The clock pulses generated triggers the SAR logic to update the register bits with data from MSB to LSB order. With each pulse, the input voltage and the DAC output voltage are compared in order to converge to the input signal.

The pulse generator makes sure that the different blocks of SAR ADC are synchronized properly which provides accurate timing and sequential conversion.

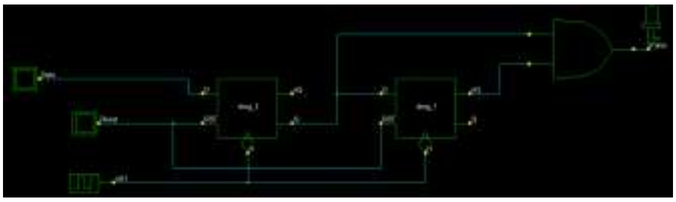

Fig : Pulse Generator .SCH File

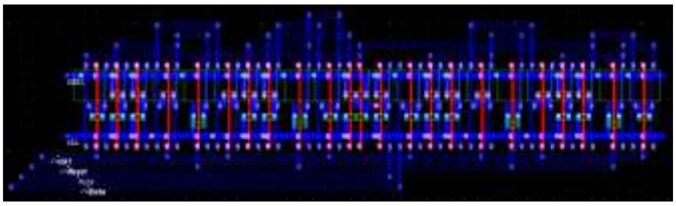

Fig : Pulse Generator.Verilog File

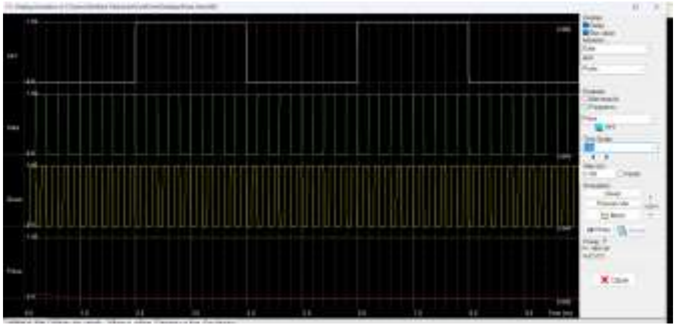

Fig : Output Waveform of Pulse Generator

### E) 4 Bit Register

In the course of the conversion process, the 4-bit register of the SAR logic circuit stores the digital output. The intermediate and final digital values produced by the SAR algorithm are stored in it.

A register is an arrangement of flip-flops for storing data. This design consists of 4 D flip-flops connected in parallel to form a 4-bit register. Each D flip-flop can store 1 bit. This means the data will shift in on every pulse in synchronisation to the clock.

SAR logic updates the bits in the register sequentially during the conversion process. At first, the most significant bit is logic ‘1’ and the DAC provides its corresponding output voltage. Based on the output from the comparator, the SAR logic decides to keep the bit ‘1’ or to reset it to ‘0’. The above procedure is repeated for all four bits till the final digital output is achieved.The four-bit register is responsible for storing the intermediate conversion results, updating the bits during the SAR operation, and generating the final digital output code.

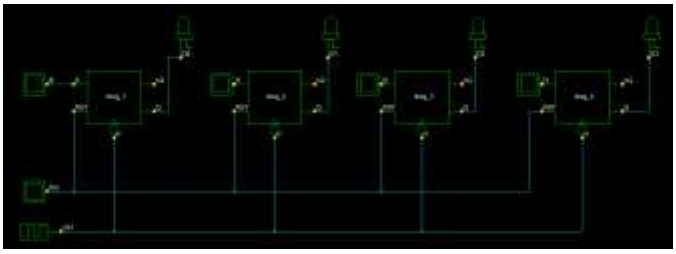

Fig : 4 Bit Register .SCH File

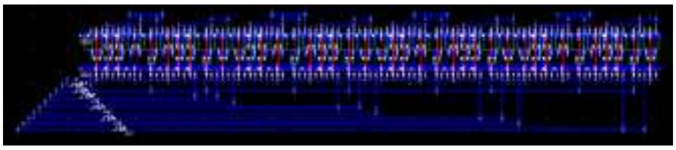

Fig : 4 Bit Register .Verilog File

Fig : Output Waveform of 4 Bit Register

**6. Future Scope**

In this paper, SAR ADC architecture utilizing CMOS technology is presented. Nevertheless, in the future study, many developments and enhancements must be investigated to further improvement performance and efficiency of the system.

In future work, it can be implemented in a more advanced CMOS technology node, which will help bring down power consumption, chip area and propagation delay with an overall faster conversion.

The converter's resolution can also be increased by increasing the number of bits in the SAR logic and the DAC architecture. Higher resolution SAR ADCs find use in applications that need increased accuracy like biomedical instrumentation and precision sensor systems.

A better design of a low-power comparator structure and use capacitor-based DAC architectures instead of resistor-based DACs can help minimize static power consumption for better energy efficiency.

Moreover, the entire SAR ADC system has the potential to be implemented on System-on-Chip (SoC) platforms for various applications, which include the Internet of Things (IoT), wireless communication systems, and embedded sensor interfaces.

Future research may also include hardware fabrication and real-time testing to evaluate the practical performance of the proposed SAR ADC design under real operating conditions.

**5. Conclusion**

In this work, a CMOS Successive Approximation Register (SAR) Analog-to-Digital Converter was successfully designed and analyzed using DSCH 3.9 and Microwind 3.9 tools based on 0.45 µm CMOS technology. The proposed architecture consists of four main functional blocks: a Sample and Hold circuit, dynamic latch comparator, R–2R ladder DAC, and SAR logic circuit.

The Sample and Hold circuit effectively captured and maintained the input analog signal during the conversion process. The dynamic latch comparator provided fast and reliable comparison between the sampled input voltage and the DAC output voltage. The R–2R ladder DAC, implemented with resistor values R = 10 kΩ and 2R = 20 kΩ, successfully generated accurate analog voltages corresponding to the digital input codes. The SAR logic controlled the conversion process using a successive approximation algorithm to produce the final digital output.

Simulation results verified the correct operation of each block as well as the complete SAR ADC system. The integration of all modules demonstrated efficient analog-to-digital conversion with a compact circuit structure and low power operation.

The results confirm that the proposed SAR ADC architecture is suitable for mixed-signal applications requiring efficient and reliable analog-to-digital conversion.

**6. Results**

A 4-bit successive approximation register (SAR) analog-to-digital converter was designed and analyzed using circuit-level simulations. The architecture consists of a sample-and-hold unit, a comparator, SAR control logic, and an R-2R ladder-based DAC. The circuit was operated with a supply voltage of 1.2 V and a reference voltage of 1.0 V. To verify its functionality, a constant input voltage of around 0.5 V was applied at the input stage. During operation, the SAR logic performs bit-by-bit approximation by comparing the input signal with the DAC-generated voltage at each step.

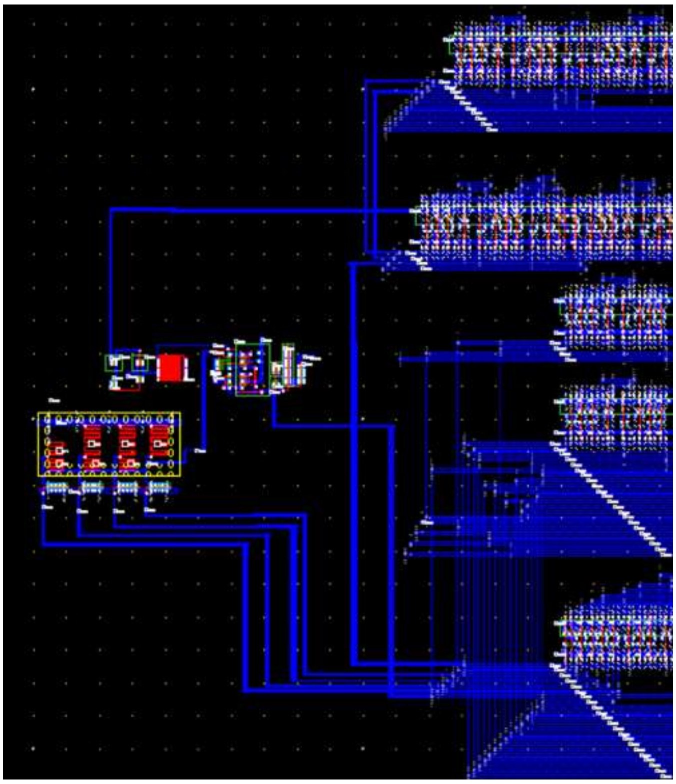

Fig : SAR ADC Connections .MSK File

Based on the simulation results, the converter produced a digital output of 0111 for the given input, which aligns well with the expected quantization level for a 4-bit system. The DAC output waveform shows a stepwise progression approaching the input voltage, indicating correct convergence behavior. Some non-ideal effects, such as slight variations in signal levels due to loading, were observed; however, they did not significantly affect the overall performance. These results confirm that the designed SAR ADC performs the intended analog-to-digital conversion effectively and can be considered suitable for low-power mixed-signal applications.

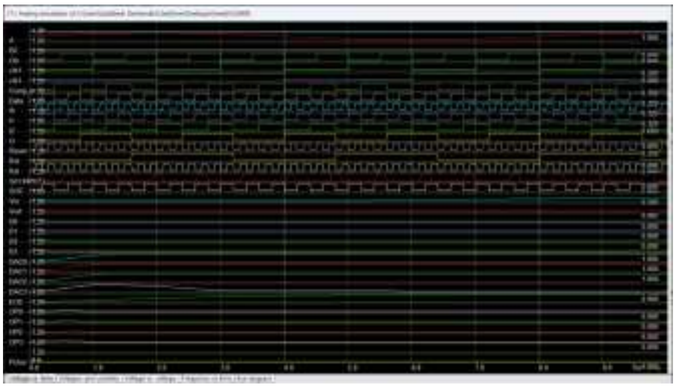

Fig : Output Waveform of SAR ADC

## 7.REFERENCES

[1] D. M. Ellaithy, “A low-power 8-bit 1-MS/s single-ended SAR ADC in 130-nm CMOS for medical devices,” Journal of Electrical Systems and Information Technology, vol. 11, p. 21, 2024, doi: 10.1186/s43067-024-00147-z.

[2] S. Li, Z. Yang, and T. Iizuka, “An All-Standard-Cell-Based Synthesizable SAR ADC with Inverter-Cell-Based Capacitive DAC,” Circuits, Systems, and Signal Processing, vol. 44, pp. 2956–2978, 2025, doi: 10.1007/s00034-024-02963-0.

[3] M.-T. Shiue, Y.-F. Lo, and C.-Y. Jung, “Design of an Internal Asynchronous 11-Bit SAR ADC for Biomedical Wearable Application,” Electronics, vol. 13, no. 17, p. 3549, 2024, doi: 10.3390/electronics13173549.

[4] D. Wang, J. Hu, X. Huang, and Q. Zhong, “Design of a 12-Bit SAR ADC with Calibration Technology,” Electronics, vol. 13, no. 3, p. 548, 2024, doi: 10.3390/electronics13030548.

[5] K. Park, S. Lee, and J. Kim, “A 12-Bit SAR ADC with Binary Search Calibration Algorithm for a Split Capacitor,” Electronics, vol. 13, no. 2, p. 414, 2024, doi: 10.3390/electronics13020414.

[6] X. He, W. Qiao, X. Xing, and H. Feng, “Inverter-based noise-shaping SAR ADC for low-power applications,” Microelectronics Journal, vol. 139, p. 106094, 2024, doi: 10.1016/j.mejo.2024.106094.

[7] X. Tang, J. Liu, Y. Shen, and S. Li, “Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 11, pp. 4468–4482, Nov. 2022, doi: 10.1109/TCSI.2022.3198465.

[8] M. Firlej, T. Fiutowski, M. Idzik, and J. Moron, “Ultra-low power 10-bit 50–90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs,” arXiv preprint, arXiv:2312.14592, Dec. 2023.

[9] Z. Hu, “Research on the Design of Low-Power SAR ADC for Wearable Health Monitoring Devices,” EWA Direct Proceedings, 2025. [Online].

[10] F. Yang, D.-H. Bui, Y. Zhao, L. Qi, J. Zhang, X.-T. Tran, and Y. Li, “Understanding Synthesizable Design Methodologies for Mixed-Signal SAR ADC Circuits,” Integrated Circuits and Systems, vol. 10, no. 2, pp. 112–121, 2025. [Online].