

Ultra-Low Power, Area Optimized CMOS Successive Approximation Based ADC for Mixed-Signal Systems

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Abstract - Analog signals are present everywhere in the form of sound or sensor readings. But today's digital systems, like microcontrollers and processors, can only work with binary numbers. For this we use analog-to-digital converters. Among the various ADC architectures, Successive Approximation Register (SAR) ADCs are widely preferred due to their low power consumption, small area, and moderate speed. However, existing SAR ADC designs still face major challenges such as high-power consumption, layout capacitor mismatch, and the requirement for stable reference voltages. These problems limit their accuracy, efficiency, and practical use in advanced applications. This Paper resolve these issues by designing four key blocks of a SAR ADC: a sample-and-hold circuit, comparator, SAR logic, and reference DAC. This Paper goal was to make the layout smaller and reduce power usage, while still ensuring accurate conversion.

Key Words: SAR Logic, Comparator, DAC, Low Power, Mixed Signal Systems

1.INTRODUCTION

Today's smartphones, medical wearables, and IoT sensors all rely on processing real world signals, whether sound, temperature, or body signals. These signals are mechanical signals, but digital systems cannot understand mechanical data. Analog-to-Digital Converters make sure the signals are converted to digital so they can be interpreted and processed in the computer. We have Flash ADCs, Pipeline ADCs, Sigma Delta ADCs, Successive Approximation Register (SAR) ADCs, and many more types of ADCs. Each type has its own advantages and drawbacks. Flash analog-to-digital converters offer very fast performance but at a high cost. Pipeline ADCs are also fast but need complex calibration. Sigma-Delta ADCs provide high accuracy but work slowly. Successive approximation register (SAR) converters act as an important link between real-world analog signals and the digital processing domain. They are often chosen in

practical designs because they can achieve useful levels of resolution while keeping energy demands low, which makes them suitable for portable and low-power systems. As a result, they are the best choice for low-power medium speed applications. In recent years, there are many advancements in SAR ADC design. Researchers focused on eliminating power consumption, saving silicon area, increasing precision, etc. Early techniques like monotonic switching, merged capacitor switching, and VCM-based steering helped to reduce power consumption effectively. Recently, SAR ADC performance has improved due to hybrid switching methods, calibration circuits, and smaller CMOS technologies. Due to these attributes, SAR ADCs have become popular in portable electronics, IoT, biotech implants, and industrial automation. Flash ADC - not used because of high power area need Pipeline ADC - Stable but less dominant in low-power systems. Sigma-Delta ADC - Still used for high-precision, but niche SAR ADC - Rapidly growing from and becoming the most dominant ADC type due to low power, compact area, and good resolution. Even with their

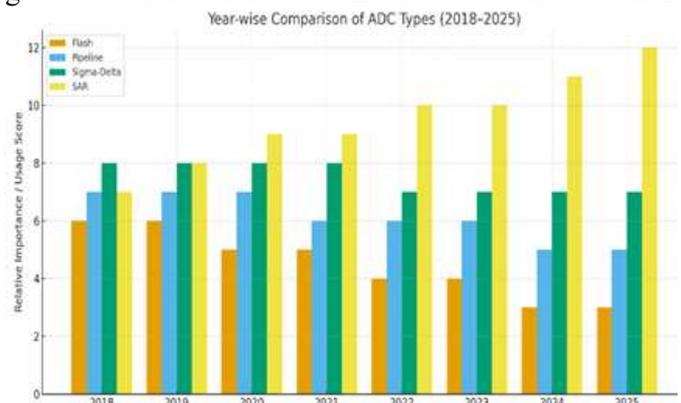


Fig 1: Year-wise bar graph (2018–2025) comparing different ADC types (Flash, Pipeline, Sigma-Delta, SAR) based on their relative importance in research and applications)

designing SAR ADCs is not straightforward. The main elements—such as the comparator, DAC, sample-and-hold unit, and control logic—interact in complex ways. Each block adds its own limitations, and achieving the desired overall performance requires carefully balancing

these constraints. This paper provides a review of ADC architectures with a special focus on SAR ADCs, summarizing key advancements, identifying existing challenges, and highlighting future research directions to achieve ultralow-power and area optimized CMOS SAR based ADC for mixed signal system.

2. Overview

The design of ADC is important for mixed-signal system performances. Mixed-signal systems typically consist of analog interfaces and a digital processing unit on a single chip. The increasing craze of wearables, IoT nodes, biomedical implants, portable communication systems has created the need for converters that consume ultra-low power, occupy tiny silicon area but still provide decent resolution and speed. The best architecture that has come up in this case is the SAR ADC. A SAR ADC requires only one comparator and a capacitor based DAC. This makes SAR ADCs more energy efficient than Flash and Pipeline architectures. The conversion process uses a binary search algorithm. In this algorithm, the input signal is sampled. After that, it is compared to a number of reference voltages. The reference voltages are generated by DAC. This step-by-step approximation removes the need for large arrays of comparators or complex multi-stage pipelines, which greatly reduces power and chip area. The digital SAR logic can scale with CMOS technology, making the architecture suitable for future technology nodes. A lot of effort is being put towards improving the DAC switching mechanism for ultra-low power. Traditional switching techniques require substantial energy because of frequent charging redistribution in the capacitor array. Designing a high-performance class d power amplifier using an enhanced modulator for accurate pulse-width modulation. With these methods energy reductions can be as much as 90% compared to the conventional one which helps in achieving femtojoule-per-conversion-step in a SAR. In addition, dynamic comparators are employed, which only consume current during the comparison phase, further reducing static power consumption. Another important consideration for mixed-signal systems is area optimization SAR ADC design. The capacitor DAC takes up most of the ADC area, especially in high resolution designs. Techniques like segmented capacitor arrays, capacitor scaling, and layout-aware matching have been introduced by researchers to reduce silicon area without compromising on accuracy. However, these methods come with challenges of capacitor mismatch and parasitic effects, which can hurt linearity. To avoid this complication, most recent SAR ADCs now use background calibration, which

can automatically correct for any mismatch and comparator offset during normal operation. Ultra-low power area efficient SAR ADCs have a lot of applications. ADC for implantable and wearable sensors in biomedical systems, for example, should consume as little energy as possible to prolong battery life, or enable energy harvesting. IoT devices use SAR ADCs to access data from physical sensors. Energy efficiency determines how long the system will last. In communication systems, SAR ADCs are integrated analog-to-digital converters which act as front ends to any communication circuit. Despite these advances, several challenges remain. It remains challenging to keep linearity and high ENOB while continuously shrinking the size of the capacitor. Moreover, achieving a sub-femtojoule energy per conversion-step across process, voltage, and temperature variations remains an open research problem. Moreover, design and calibration must consider the non idealities of the sample-and-hold circuit and the mismatch in the scaled CMOS processes. In conclusion, the ultra-low power and area-optimized SAR ADC stands out as the leading candidate for mixed-signal systems in advanced CMOS technology. Its balance of efficiency, compactness, and adaptability makes it highly suitable for emerging low power applications. Ongoing research continues to address the challenges of mismatch, noise, and scaling effects, with the ultimate goal of delivering converters that achieve robust, sub-femtojoule energy performance in real silicon implementations.

3. Problem Statement

The advanced mixed-signal systems with portable devices need ADCs with low power and area. Among all architectures, it is the Successive Approximation Register ADC which has come out to be the most suitable because it offers a good tradeoff between resolution, power consumption and integration in CMOS technology. Challenges remain in designing SAR ADC in advanced technology nodes despite its advantages. The Sample-and Hold (S/H) circuit suffers from charge injection, clock feedthrough, leakage, and thermal noise that degrade accuracy and reduce effective resolution. Furthermore, the capacitor-based DAC, which is the biggest contributor of power and silicon area to the ADC, suffers from mismatch and parasitic effects at deep-submicron nodes causing large non-linearity errors. Researchers have come up with energy efficient switching scheme and calibration scheme to tackle these issues; however, most of the solutions either make the circuit complex, require more area or do not remain robust over PVT. Therefore, the main problem tackled in this work is the design and

optimization of a Sample-and-Hold circuit and DAC of a SAR ADC implemented in CMOS. The aim is to achieve low power and small silicon area while accepting resolution and accuracy and hence making the design suitable for modern mixed-signal.

4. Proposed Work

The project Ultra-low power, area optimized CMOS Successive approximation based ADC for mixed signal systems, designing in MICROWIND and DSCH Software. The block diagram is as follows: These mainly consist four blocks for designing purpose that is Sample and Hold Circuit which is basically frontend of This Paper. Then comparator comes in picture which convert analog signal to digital signal and another one is successive approximation register and Digital to Analog converter.

Sample And Hold Circuit : Sample and hold circuit is frontend of a circuit. It is an important block in an ADC that captures the instant value of an analog input signal during the sampling phase and holds it steady during the conversion phase. One of the most efficient and widely used implementations of the S/H circuit is based on a transmission gate switch combined with a CMOS.

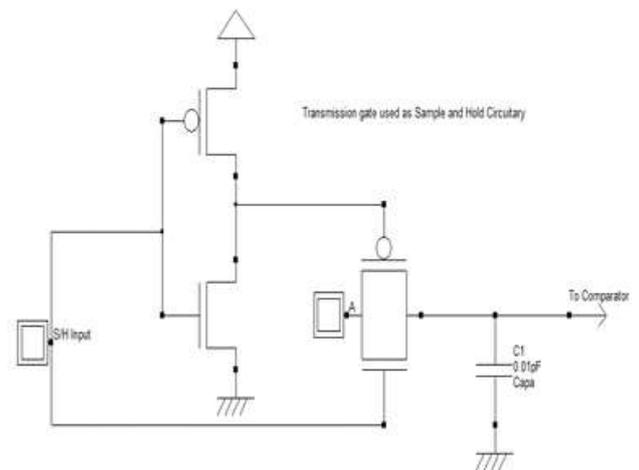


Fig 3. Transmission gate based Sample and Hold Circuit.

The Sample and Hold (S/H) circuit is the very first stage of our SAR ADC design. Its role is simple but very important: it captures the instantaneous value of the analog input signal and keeps it stable while the rest of the ADC finishes the conversion. Without this block, the input would continue to change while comparison is taking place, which would result in errors. The circuit works in two phases: the sampling phase and the hold phase. In the sampling phase, a switch connects the input signal to a capacitor. The capacitor charges up to the current value of the input. In the hold phase, the switch turns off, disconnecting the input. The capacitor then “remembers” that voltage for a short period of time. This fixed value is then passed on to the comparator and DAC, ensuring they always work on a steady signal during bit-by-bit decisions. While the idea is simple, the design needs careful choices: Capacitor value: If the capacitor is too small, random noise (kT/C noise) becomes large and affects accuracy. If it is too large, charging takes longer and the circuit may not settle before conversion starts. So, a balanced value is chosen — small enough for speed, but large enough to reduce noise well below one LSB of the ADC. Switch design: A single MOS switch introduces charge injection when it turns off, which slightly changes the stored voltage. To minimize this error, a transmission gate (NMOS and PMOS in parallel) is used. This allows better linearity and reduces unwanted charge effects. Three main non-idealities affect the performance of this block: 1. Charge injection – occurs when carriers are released into the capacitor during switching. 2. Clock feedthrough – switching signals couple into the hold capacitor through parasitic capacitances. 3. Thermal noise (kT/C noise) – noise generated due to finite capacitance size. Each of these was considered during design. Using a transmission gate, bottom-plate sampling, and proper

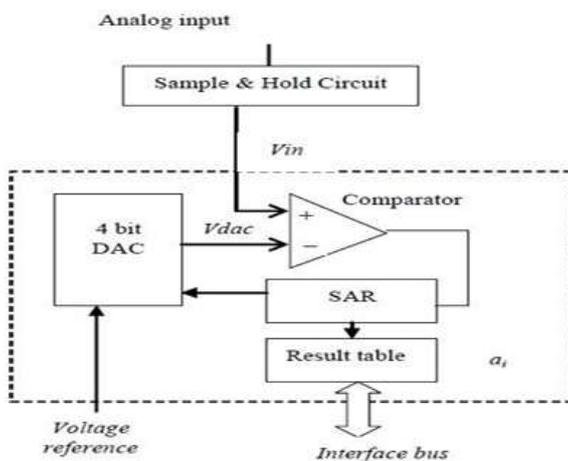


Fig 2: Block diagram of ADC

Fig.2 Block Diagram of ADC

hold capacitor and a buffer amplifier. The transmission gate is made by combination of NMOS and PMOS placed in parallel direction, controlled by complementary clock signals. So, it overcomes the limitations of a single MOS transistor like threshold voltage drop and signal distortion when passing analog signals. By using both PMOS and NMOS the transmission gate achieves nearly ideal switching characteristics, providing low on resistance.

sizing reduces the first two errors. For noise, capacitor sizing was chosen so that the noise level remains much lower than the ADC resolution. In the layout (designed in Microwind), the capacitor is placed close to the comparator input to avoid extra routing capacitance. The transmission gate is drawn symmetrically to ensure balanced operation, and dummy devices are added to reduce mismatch. Guard rings are used to shield the circuit from noise coming from the digital blocks. The S/H block was tested through transient simulations. A slowly varying input was sampled to check how accurately the capacitor holds the value. The droop in the held voltage was measured and found to be within acceptable limits. The settling time was verified to make sure the capacitor charges quickly enough within the sampling window. Tests also confirmed that charge injection errors remain small when the transmission gate is used. This block is crucial for overall ADC accuracy. If the Sample and Hold is not designed properly, even the best comparator or DAC cannot fix the error. By ensuring stable and low-noise sampling, the S/H stage provides a reliable input to the comparator, making the entire conversion process more precise.

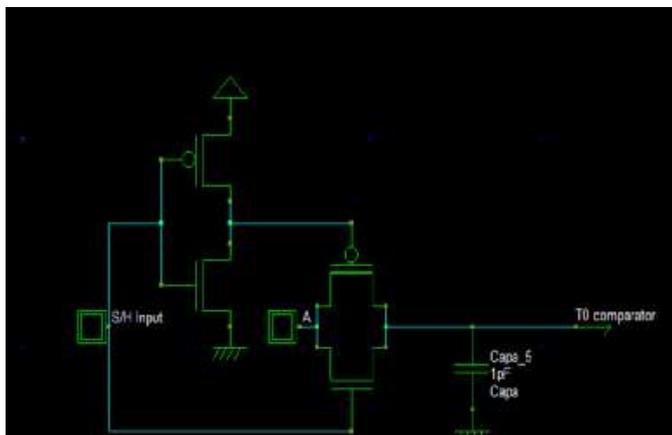


Fig 4 : Transmission based Sample and hold circuit .SCH file

From that A Verilog file is created and which is then combined in Micro wind.

```
// DSCH 3.9
```

```
//C:\Users\bhart\OneDrive\Desktop\Sample_and_hold_Circuit.sch
```

```
module Sample_and_hold_Circuit( A,SbHInput;
wire w4,w5;
nmos #(1) nmos_1(A,w4,SbHInput); // 0.3u 0.05u
pmos #(1) pmos_2(A,w4,w5); // 0.5u 0.05u
nmos #(1) nmos_3(w5,vss,SbHInput); // 0.3u 0.05u
pmos #(1) pmos_4(w5,vdd,SbHInput); // 0.5u 0.05u
capa #(1) Capa_5(vss,w4); // 1pF endmodule
```

```
//Simulation parameters in Verilog Format always
#200 A=~A;
#400 S/H Input=~S/H Input;
// Simulation parameters
// A CLK 1 1
// S/H Input CLK 2 2
```

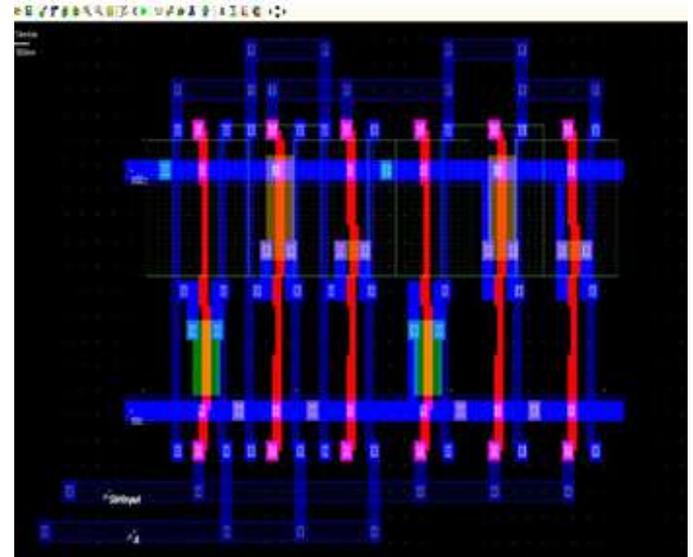


Fig 5: Compiled in Microwind

Comparator:

The comparator is the most critical and important element in a SAR ADC because it performs the actual decision step during conversion. After the input voltage is sampled and held, the comparator checks whether this voltage is greater or smaller than the value generated by the reference DAC. Its output, either logic “high” or “low” is passed to the SAR register, which updates the digital code at each step. The speed, accuracy, and power consumption of the entire ADC are strongly influenced by the performance of the comparator. In our design, the comparator is designed using 0.45 μm CMOS technology in Microwind environment, we have focused on developing a comparator that is both energy efficient and compact in layout. A dynamic latch-based comparator topology was selected, as it avoids static power consumption and operates with high speed, which makes it ideal for ultra-low-power applications. To further reduce offset and improve sensitivity, a small pre-amplifier stage is included before the latch stage. This combination allows the comparator to produce a sharp and reliable transition at the clock edge, even for small differences between the input and DAC voltages. The layout has been carefully optimized to minimize chip area, which is important for a design where compactness is a priority. Symmetry was maintained between the differential transistor pairs to reduce mismatch, as even

small offset errors could affect the limited 4-bit resolution. Simulation in Microwind confirmed that the comparator responds reliably and produces correct transitions within each approximation cycle. Recent research highlights the value of comparator improvements for SAR ADCs. For instance, a study on an 8-bit SAR ADC with an enhanced comparator in 180 nm CMOS (IJECE, 2024) demonstrated how parallel clocking in the latch stage reduced parasitic effects and achieved very low delay (~157 ps). While our design targets a 4-bit resolution and focuses more on ultra-low power and area optimization, this work supports the idea that careful comparator design directly improves the accuracy and speed of SAR ADCs. Thus, the comparator block in our 4-bit SAR ADC is optimized for low power, small area, and reliable decision-making, aligning with the overall goal of developing an ultra-low power, area-efficient ADC for applications in IoT and portable systems.

Digital to Analog converter: The Digital to Analog Converter (DAC) is an important block in a SAR ADC. Its job is to create reference voltages that are compared with the input signal during every step of the conversion. In a 4-bit SAR ADC, the DAC must generate 16 different voltage levels (from 0000 to 1111 in binary). If these voltage levels are not accurate, the ADC will not work properly. For This Paper, we used an R-2R resistor ladder DAC. This design is simple because it only needs two resistor values: R and 2R. The resistors are connected in a ladder pattern, and each bit (B0 to B3) controls a switch that connects either to the reference voltage or to ground. Depending on the binary input, the DAC gives an output voltage that represents the correct analog level. One big advantage of the R-2R DAC is that the output resistance stays the same no matter what the digital input is. This makes it easier for the comparator to work with the DAC output. It also takes less area compared to capacitor-based DACs, which is useful in This Paper where saving chip area is important. In our design we made sure that the resistors are matched and placed appropriately such that there is a proper R to 2R ratio. If the ratio is not exact, the DAC output can have errors. The DAC was tested in the Microwind 0.45 μm CMOS technology and was found to give correct and stable output voltages with negligible error. Improvements in DAC designs to help save power have been shown by others. For instance, a recent research published in Micromachines (2023) reveals a nearly 94% reduction in DAC power through optimized switching methods. Even though it was just a 4-bit project, we followed the same idea and made it simple to reduce power and area. The DAC was tested in the

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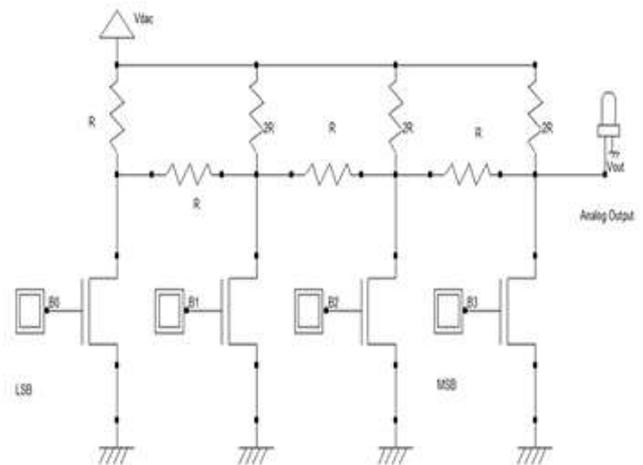


Fig.6: CMOS based 4-Bit DAC Schematic

With this R-2R DAC, our SAR ADC design can work with low power and compact area, making it suitable for IoT devices, biomedical systems, and portable electronics.

Successive Approximation Register:

The SAR ADC has a digital control unit which is a Successive Approximation Register logic. The “decision maker” which instructs the comparator and DAC to perform conversions. If this block was not present, then the working of this ADC was not possible. A 4-bit SAR ADC has a systematic operation of the SAR logic. When a conversion begins, the MSB is set to logic “1” and all the other bits to “0”. The DAC (Digital to Analog Converter) is sent this test code for reference voltage generation. The comparator checks to see if the input signal is larger than or smaller than this DAC voltage. When the input is higher, the MSB is maintained “1” otherwise, it is reset to “0”. The logic moves to the next bit after this first check after setting it to “1”, the same comparison is done. The operator does this until all four bits have been tested After four clock cycles, the SAR logic provides the final 4-bit digital output which best approximates the given input analog signal. Our design

utilises Microwind tool to implement the SAR logic using 0.45 μm CMOS technology. They use a combination of D flip-flops, shift registers and basic logic gates to update the bit decisions with the system clock. The design is compact and consumes very little power because only a small number of transistors switch during each cycle. This makes it particularly suitable for low-power systems such as IoT and portable electronics. Control signals must be timed carefully since every step of the approximation needs to happen in the right sequence was how this paraphrased. Clock pulses were used to trigger the bit updates so that only one bit is tested at a time. According to the simulation results of Microwind, it can be stated that the SAR logic is able to complete the conversion in four cycles. This is similar to the ADC with a resolution of 4-bit. A recent study also highlights SAR logic design's role in enhancing ADC performance. Research focusing on SAR ADCs with high resolution has revealed the potential of asynchronous control techniques to enhance overall conversion speed and minimize power draw. This Paper may be based on 4-bit only, but the same concepts can be extended to a higher system with the same design and control logics within the register. In general, our design features low-power, area-efficient, and reliable control mechanism for SAR logic. The sample and-hold circuit, comparator and DAC will ensure SAR ADCs's proper functioning and help us meet the project objective of ultra-low power area-efficient CMOS SAR ADCs design.

5. Future Scope

This project focused on designing a 4-bit SAR ADC using 0.45 μm CMOS technology in Microwind, with the main aim of keeping both power consumption and chip area as low as possible. While the work shows that such a compact design is achievable, the field of ADCs is very broad, and there are many opportunities to take this work further in the future. The following points highlight the areas where the design can be improved or extended.

1. Moving Towards Higher Resolution The present design is limited to 4 bits, which is suitable mainly for proof-of-concept and simple sensor applications. Future work could scale the resolution to 8, 10, or even 12 bits. A higher number of bits would allow the converter to handle signals that demand better precision, such as biomedical data or audio signals. Of course, increasing resolution would also bring challenges, particularly the need for a more accurate comparator and a DAC with tighter matching, but the methods developed here provide a good foundation for tackling those challenges.

2. Implementation in Smaller Technology Nodes This design was carried out in 0.45 μm technology. While this node is useful for learning and simulation, modern ICs are generally implemented in much smaller nodes, such as 180 nm, 90 nm, or even below. Re-implementing the design in a more advanced node would make the ADC faster, reduce power use, and shrink the silicon area even further. On the other hand, smaller nodes come with new issues like leakage currents and reduced supply voltages, which would need to be considered carefully.

3. Improved DAC Techniques In this project, the DAC was implemented in a simple structure to keep the layout compact. In future work, the DAC could be modified with energy-saving techniques like capacitor-splitting or monotonic switching, which are often used in higher-resolution SAR ADCs. Research shows that these methods can cut DAC power by more than 90%, which is valuable for battery-powered applications. Even in a 4-bit design, exploring such switching methods could improve efficiency.

4. Smarter SAR Logic Our design used synchronous SAR logic, where each bit decision is made in one clock cycle. A possible extension is to use asynchronous logic, which moves to the next step as soon as the comparator gives its output. This would make conversions faster and avoid wasting time waiting for the next clock edge. Another interesting direction is adaptive SAR logic, which changes the approximation steps depending on the signal behavior, making the ADC more flexible for applications such as bio signals or IoT sensors.

5. Applications in IoT and Healthcare

One of the strongest motivations for building a low-power, compact SAR ADC is its use in IoT and biomedical systems. Future work could focus on directly embedding this ADC into a complete system-on-chip that interfaces with sensors. For example, a wearable health monitor could use the ADC to digitize ECG or EEG signals with very little energy overhead. The 4-bit design is only the beginning; once optimized, it can be integrated with amplifiers, filters, and wireless modules to form a full system for portable devices.

6. Fabrication and Real Testing keeping both power consumption and chip area as low as possible. While the work shows that such a compact design is achievable, the field of ADCs is very broad, and there are many opportunities to take this work further in the future. The following points highlight the areas where the design can be improved or extended. 1. Moving Towards Higher Resolution The present design is limited to 4 bits, which is suitable mainly for proof-of-concept and simple sensor

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data about parameters like offset, noise, and linearity. It would also show how the design behaves under process variations, temperature changes, and other real world effects. This stage is essential for moving the design from an academic prototype to a working product.

7. Hybrid and Mixed Architectures

Another possible direction is to explore architectures that combine SAR with other ADC techniques. For example, SAR can be combined with sigma-delta modulation to achieve higher resolution without too much power overhead, or with flash ADCs for a faster coarse-fine approach. Such hybrid designs could balance power, resolution, and speed more effectively than a pure SAR architecture.

8. Design Automation and AI Tools

As ADC design becomes more complex, manual optimization of transistor sizes and layout can be time-consuming. In future, machine learning and automated optimization could be used to improve performance. Recent studies show that neural networks and analytical models can help tune comparator sizing or DAC capacitor ratios much faster than trial-and-error. Applying such methods to SAR ADCs could save time and produce better designs with less manual effort.

9. Low-Voltage Operation and Energy Harvesting Systems

With the rise of self-powered devices and energy harvesting, ADCs must be able to work at very low supply voltages, sometimes below 0.5 V. Extending this design to ultra-low voltage operation would make it useful for systems powered by ambient energy sources such as solar cells or vibration harvesters. This would require exploring circuit techniques like sub-threshold operation, body biasing, or low-swing logic.

10. Contribution to Industry and Research

Finally, the knowledge and methods developed in this project can contribute both to academic research and industry applications. In the academic setting, the design can serve as a base for student projects, further research on low power ADCs, or even publications. In industry, compact SAR ADCs are widely used in microcontrollers, mobile devices, and sensor platforms. By continuing to refine and extend this design, it could eventually meet the requirements of real commercial systems.

6. Results

After studying existing SAR ADC research, a number of clear trends emerged. Shifting energy reduction from 2010–2013 through the use of monotonic and merged capacitor switching offers a 95% power reduction over conventional SAR ADCs. But these designs still suffered

from mismatch and reference voltage stability sensitivity. Technology Scaling – SAR ADCs are scalable as it could be shown that as CMOS technology shrunk from 180 nm to 65 nm and finally to 45 nm, the ADC

could be made smaller and faster and may consume lower power per conversion step. As a case in point, 45 nm CMOS designs reached ultra-low power of 1-2 μW , which is suitable for biomedical applications. Application - Specific Designs 2022–2025 work on wearables, IoT, biomedical implants where ultra-low power is more important than very high-speed. Certain designs were able to achieve below 5 μW power consumption at biosensor sampling speeds. Another work at the advanced nodes (28 nm) demonstrated gigahertz-level sampling with reconfigurable resolution, but he does this at higher power consumption. Most works suffer from the limiting issues that only simulation results are reported from the simulation. Not many designs were fabricated and tested in silicon which leaves their real performance in doubt.

7. Conclusion

Analog-to-Digital Converter (ADC) is one of the most crucial building blocks of mixed-signal systems. The Successive Approximation Register (SAR) ADC has become the most used type of ADC because of its low power, small area, and good accuracy. It can be seen from the literature that a number of techniques which include monotonic switching, merged capacitor switching, VCM-based switching has helped in reducing power and improving energy efficiency. Recent research in advanced CMOS nodes (65 nm, 45 nm and 28 nm) has focused on wearables, biomedical devices and IoT application where saving power is more important than very high speed. Nonetheless, almost all designs have their problems, such as capacitor mismatch, need an accurate reference voltage, and very limited tests on real hardware. Although the results of the simulation show excellent efficiency, a practical design that combines low power, small area accuracy, and stability system is not yet available. Modern low-power solutions to early switching techniques of SAR ADCs are observed in this paper. The results indicate that although a lot has already been done, there is still further room for energy-efficient, rugged designs to fill in the gaps in real applications. Next generation electronic devices will have enhanced demand on ADCs. Future work on such applications will involve calibration techniques, silicon testing, and integration into compact low power systems.

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