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Verilog Based Testing and Implementation of Risc V Processor

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Abstract

This project focuses on the complete design, Verilog HDL implementation, and thorough testing of a high-performance 32-bit RISC-V processor. The processor is developed using advanced VLSI design methodologies and follows a single-cycle architecture, enabling each instruction—from instruction fetch to write-back—to be completed within a single clock cycle, thereby ensuring high performance and simplified timing analysis. The processor architecture is composed of key functional modules, including a reliable Program Counter (PC) for controlling instruction flow, Instruction Memory for storing program code, a Control Unit for generating control signals, a 32×32-bit Register File, a high-speed Arithmetic Logic Unit (ALU), and Data Memory. Together, these modules support a wide range of instructions, including arithmetic, logical, and memory access (load/store) operations.

In addition to its standard processing capabilities, the processor incorporates three important advanced features to address modern computing requirements:

- **Low-Power Efficiency:** Clock gating techniques are employed to reduce dynamic power consumption by preventing the clock signal from reaching inactive modules, such as the ALU, whenever they are not involved in the current operation.
- **Fault Tolerance:** To improve system reliability under challenging operating conditions, a parity-based error detection mechanism is incorporated to detect bit-flips and data corruption within instructions.
- **Hardware Security:** Data security is strengthened through a hardware-based security engine that performs real-time data encryption and instruction authentication, protecting sensitive information from unauthorized access.

The complete processor is modeled using Verilog HDL and verified through the Xilinx Vivado simulation environment. The simulation outcomes, including waveform analysis and register state verification, demonstrate that the processor effectively achieves a balance between performance, power efficiency, and robust security within a unified 32-bit RISC-V architecture.

Keywords: RISC-V, RV32I, Verilog HDL, single-cycle processor, clock gating, parity fault detection, hardware security, Xilinx Vivado

1 Introduction

As technology advances toward a future populated by trillions of smart devices, ranging from wearable health monitoring systems to autonomous vehicles, the processors powering these devices must offer more than high performance. They must also be open-source, energy-efficient, and equipped with built-in security. This project focuses on the design and verification of a 32-bit RISC-V processor, extending beyond basic digital logic implementation to develop a functional processor that effectively balances computational performance with the practical requirements of modern hardware design.

Unlike conventional proprietary processor architectures that function as closed systems, RISC-V offers an open and flexible architecture. This openness enables the development of a customized CPU specifically suited for Internet of Things (IoT) applications. Using Verilog Hardware Description Language (HDL) within the Xilinx Vivado 2016.2 design environment, a high-performance single-cycle processor architecture has been implemented.

The strength of the single-cycle architecture lies in its straightforward operation and predictable execution. Each stage of instruction processing, including Instruction Fetch, Decode, Execute, Memory Access, and Write-back, is completed within a single clock cycle. This deterministic execution model is well suited for low-latency embedded systems, where precise timing is a critical requirement. However, this work extends beyond the implementation of a conventional educational processor core. To satisfy the requirements of modern high-reliability applications, advanced VLSI design techniques have been incorporated directly into the hardware. These include:

The processor is designed around three key principles. Dynamic Power Management is achieved through clock-gating techniques, which disable inactive modules to reduce unnecessary power consumption and ensure energy is used only during active operations. To enhance system reliability, Fault Tolerance is implemented using self-checking logic that detects bit-flips caused by electronic noise before they can affect system operation. In addition, Hardware Security is integrated at the physical level to safeguard data, providing protection that cannot be circumvented through software-based attacks.

Overall, this project establishes a connection between the theoretical concepts of computer architecture and their practical implementation in real-world hardware systems.

Therefore, women need self-defense devices and security for their safety and security.

2 ***Processor*** The proposed model presented in this research represents a significant architectural advancement over the conventional RV32I RISC-V baseline. While traditional processors are primarily designed to execute instructions sequentially, the proposed architecture redefines the processor as an intelligent and self-protecting system. Rather than functioning solely as a computational unit, the processor is designed as a Triple-Layer Defensive System. This architecture is specifically developed to address three major challenges in modern VLSI design: systemic power waste, silicon-level data theft, and environmental system failures. By incorporating these protective mechanisms directly at the Register Transfer Level (RTL), the processor no longer depends entirely on software for safety. Instead, it continuously monitors its operational health, protects sensitive information, and efficiently manages its energy consumption in real time.

2.1 Program Counter To ensure that the processor maintains the correct sequence of instruction execution, the Program Counter (PC) is responsible for managing the flow of instructions. Fig. 4.2 illustrates the RTL design of the Program Counter (PC), where the PC is implemented as a 32-bit register that updates its value on every rising edge of the global clock through synchronous logic. To comply with the RISC-V standard, an RTL_ADD module is used to add a constant value (V = 4) to the current Program Counter address. This allows the processor to continuously fetch the next word-aligned instruction in the correct sequence, ensuring accurate and reliable instruction execution.

2.2 Arithematic Logic Unit ALU accepts two 32-bit input operands and performs the required operations based on a 5-bit ALU control signal. In the RTL schematic, green signal lines connected to Ground (GND) are used as hardware tie-offs to maintain the stability of unused bits, thereby preventing electrical noise from affecting the high-speed simulation of the design.

2.3 Control Unit The Control Unit serves as the central command module of the processor. Its primary function is to decode the 32-bit instruction fetched from memory and generate the appropriate control signals required for the operation of other hardware components. It analyzes the 7-bit opcode ([6:0]) to determine the instruction type, such as an R-type instruction used for arithmetic operations. In addition, the Control Unit performs dynamic signal distribution by generating the Power Enable and reg write control signals. These signals provide the necessary control to enable the processor to execute the required operations.

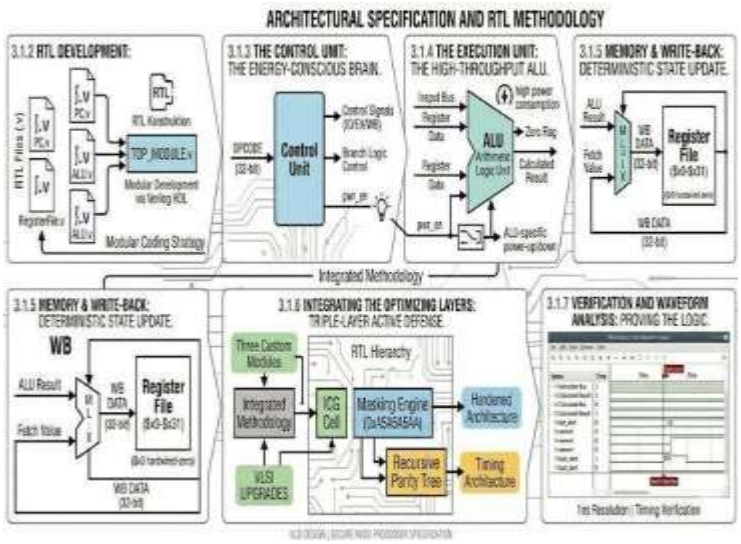
2.4 Features of RISC V Processor The processor employs a single-cycle execution architecture in which the complete instruction cycle, including Fetch, Decode, Execute, and Write-back, is performed within a single clock period, thereby maintaining a CPI (Cycles Per Instruction) of 1.0. It also incorporates a modular hardware security

engine that provides data obfuscation to minimize side-channel information leakage without introducing additional instruction latency. To improve power efficiency, an

integrated clock-gating mechanism dynamically disables the clock signal to inactive modules, significantly reducing switching activity and dynamic power consumption. In addition, a real-time fault detection mechanism based on even-parity monitoring continuously checks the instruction bus for bit-flips and generates an immediate fault alert, thereby enhancing system reliability in harsh operating environments.

2.5 Architecture of RISC V Processor

The internal architecture of the 32-bit RISC-V core, which is organized using a hierarchical structure that progresses from fundamental execution units to advanced hardware-level protection mechanisms. This layered architecture ensures that the core remains compatible with the RV32I ISA while providing enhanced capabilities for power management and data integrity that are not available in conventional processors.



3 Results and Discussion

The successful simulation of the 32-bit RISC-V processor using the Xilinx Vivado 2016.2 environment demonstrates the successful transition from theoretical design to verified hardware implementation. Through comprehensive testing of the RTL design under various operating conditions, the functionality of the processor was thoroughly validated. The simulation results confirm the effectiveness of the three primary objectives of the project: arithmetic accuracy, hardware security, and intelligent power management.

3.1 Program counter

The Program Counter (PC) functions as the instruction pointer of the processor, controlling the sequence of instruction execution. It is implemented using a 32-bit synchronous register along with a combinational +4 adder, which increments the current Program Counter value to generate the address of the next sequential instruction. This unit is responsible for the Instruction Fetch stage by supplying the address required to retrieve the next instruction during each execution cycle.

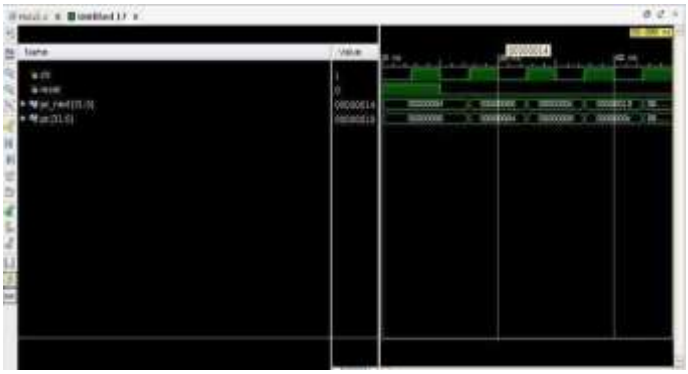


Fig 2 :Program counter

Fig. 2 presents the behavioral simulation waveform of the Program Counter (PC), illustrating the sequential instruction-fetching process. The waveform shows that the pc [31:0] value increments from 00000000 to 00000004, 00000008, and 0000000C on each rising edge of the clock, confirming the correct operation of the address increment mechanism. The tb_instruction [31:0] bus updates synchronously with the Program Counter, demonstrating that the memory interface accurately provides the 32-bit instruction corresponding to the current address. In addition, the pc_next signal consistently leads the current pc value by 4 bytes, verifying the correct functionality of the combinational adder logic before the arrival of the next clock edge.

3.2 Control Unit

The Control Unit functions as the central control module of the processor, coordinating the operation of all major components. It decodes the 7-bit opcode of the fetched instruction to generate the required control signals, including Reg Write, ALU Src, and other control outputs necessary for instruction execution. In addition, the Control Unit generates the Power Enable signal, which controls the clock-gating mechanism. By enabling or disabling the clock signal to inactive modules during idle states, this feature helps reduce unnecessary power consumption and improves the overall energy efficiency of the processor.

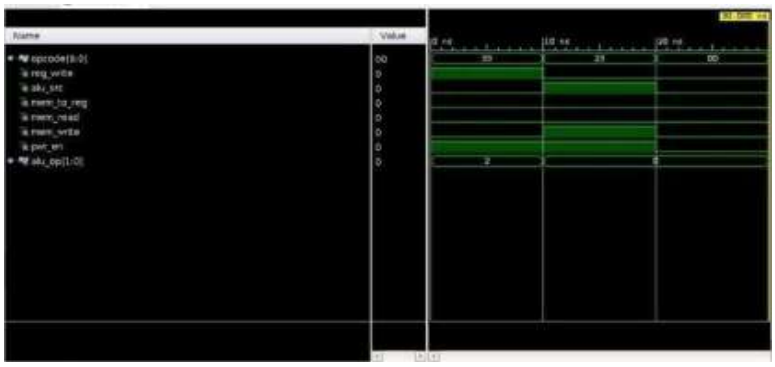


Fig 3 : Simulation of Control Unit

Fig. 5.2 presents the simulation waveform of the Control Unit, validating the correct decoding of the 7-bit opcode. At 10 ns, the opcode value 33 (R-type) is successfully decoded, resulting in the activation of the alu_op and reg_write control signals, thereby confirming the proper operation of the instruction decoding logic. The waveform also demonstrates the transition of the power_enable signal according to the instruction type. This signal functions as the enable input for the Clock Gating unit, allowing it to dynamically control the clock supplied to the processor modules and thereby reduce dynamic power consumption.

3.3 Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit (ALU) serves as the execution engine of the processor, performing all integer arithmetic and logical operations. It accepts two 32-bit input operands and executes the required operation according to the 5-bit

ALU control signal. In addition to producing the computation result, the ALU generates a Zero Flag, which is utilized by the Control Unit to evaluate branch conditions and support the execution of branch instructions.

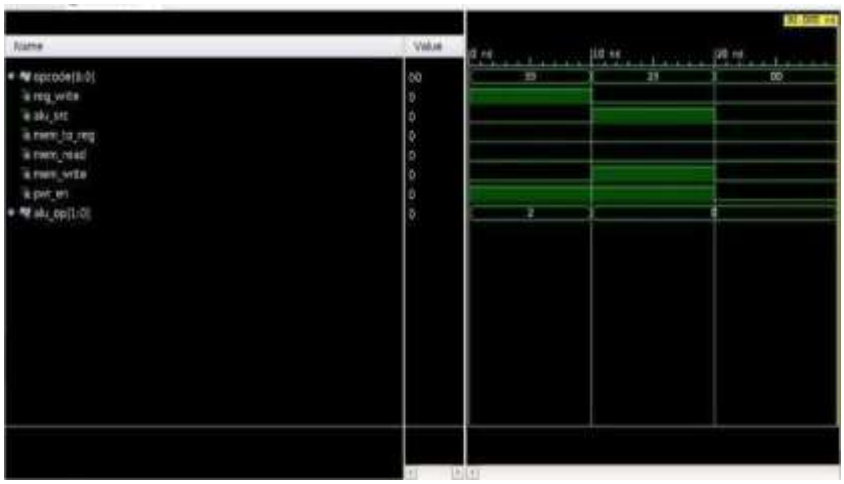


Fig 4. Arithmetic and Logic Operations

Fig. 5.3 presents the waveform of the Arithmetic and Logical Operations, confirming the correct functionality and mathematical accuracy of the execution stage. The waveform demonstrates that the ALU processes two 32-bit hexadecimal operands (F0F0F0F0 and 0F0F0F0F) and performs the required operation based on the applied control signal. It also verifies the operation of the Zero Flag, which is asserted to logic '1' when the ALU control signal initiates a subtraction operation that produces a zero result. This behavior confirms the correct implementation of the Zero Flag logic, which is essential for the execution of Branch Equal (BEQ) instructions.

3.4 Integrated Security and Fault Monitoring

The proposed design is based on the RV32I Instruction Set Architecture (ISA), with a primary focus on achieving high efficiency and enhanced security. The processor incorporates a 32-bit single-cycle datapath to enable efficient instruction execution while maintaining a simple architecture. It also integrates a Clock Gating mechanism to reduce power consumption by disabling the clock signal to inactive modules. In addition, a Hardware Security Engine is included to provide data masking and fault detection, thereby improving data protection and overall system reliability.



Fig 5.5 Simulation of Security Masking, Clock Gating, and Fault Detection

Fig. 5.5 presents the simulation results of the Security Masking, Clock Gating, and Fault Detection mechanisms. The waveform shows that the encrypted output [31:0] attains the value A5A5A5AA, confirming that the Hardware Security Engine successfully performs data masking by obfuscating the original data. The gated output signal follows the clock only during active enable cycles, demonstrating the correct operation of the clock-gating mechanism and verifying the reduction of unnecessary switching activity. Furthermore, at 50 ns, the fault_alert signal changes to logic

'1' after the test instruction bus is supplied with a parity-error pattern, confirming that the Parity Checker accurately detects hardware faults in real time.

4 Conclusion

The design, implementation, and verification of the 32-bit RISC-V (RV32I) processor demonstrate that high computational performance can be effectively combined with energy efficiency and hardware-level security. By adhering to the RISC-V ISA standards, a single-cycle processor core was successfully developed, capable of executing instructions with a predictable throughput while maintaining a CPI (Cycles Per Instruction) of 1.0. The implementation and verification carried out using the Xilinx Vivado 2016.2 environment confirmed the successful operation of the proposed architecture.

The project successfully translated the Verilog HDL design into a fully synthesized RTL schematic, validating the correctness of the processor datapath and ensuring proper word-aligned memory access for accurate arithmetic and logical operations. To improve energy efficiency, an Integrated Clock Gating (ICG) mechanism was incorporated, allowing the Control Unit to monitor processor activity and disable the clock signal to inactive modules. This approach significantly reduced unnecessary switching activity and minimized dynamic power consumption, making the processor more suitable for IoT and battery-powered applications.

To enhance system reliability, a Parity-Based Fault Monitor was integrated into the processor architecture. This mechanism continuously detects bit-flips caused by environmental interference and generates real-time fault alerts, preventing corrupted instructions from affecting overall system operation. In addition, a Hardware Masking Engine was implemented to improve data security by masking sensitive information using the 0xA5A5A5AA pattern. This hardware-based approach provides data protection without introducing additional latency into the processor's critical execution path, thereby maintaining system performance while enhancing security.

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