INTERNATIONAL JOURNAL OF SCIENTIFIC RESEARCH IN ENGINEERING AND MANAGEMENT (IJSREM)
VOLUME: 10 ISSUE: 10 | OCT - 2026 SJIF RATING: 8.659 ISSN: 2582-3930

Verilog HDL-Based Simulation Framework for Multi-Parameter Industrial Motor Fault Classification

Nagarjuna Tanikonda
Department of Electronics and Communication Engineering
CMR Technical Campus
Hyderabad,India
nagarjuna.ece@cmrtc.ac.in

K.Sravya
Department of Electronics and Communication Engineering
CMR Technical Campus
Hyderabad,India
konthamsravya05@gmail.com

A.Rishitha
Department of Electronics and Communication Engineering
CMR Technical Campus
Hyderabad,India
Avularishitha12@gmail.com

K.Vivek Rao
Department of Electronics and Communication Engineering
CMR Technical Campus
Hyderabad,India
abc@gmail.com

G.Dilip Kumar
Department of Electronics and Communication Engineering
CMR Technical Campus
Hyderabad,India
dilipguduru1215@gmail.com

Abstract— Industrial motor faults can lead to operational downtime and increased maintenance requirements, making fault monitoring and classification important for reliable motor operation. This paper presents a Verilog HDL-based simulation framework for multi-parameter industrial motor fault classification. The framework models six motor-condition parameters—motor current, vibration, temperature, rotor flux, stator flux, and supply voltage—under predefined normal and fault conditions. The proposed design adopts a modular structure comprising motor signal generation, feature processing, rule-based classification, and a 3-bit fault-code generator. The design was compiled and simulated using Icarus Verilog, while Value Change Dump (VCD) files and GTKWave were used for waveform-level verification. The framework defines healthy, rotor, stator, bearing, voltage, and overload conditions using fault codes from 000 to 101. The documented simulation demonstrates the classification of healthy, rotor, stator, bearing, and voltage-fault conditions using the corresponding encoded outputs. The simulation results provide waveform-level evidence of the classification behavior under the predefined test conditions. The proposed framework is limited to HDL simulation and provides a basis for future extension to measured motor signals, FPGA implementation, and more advanced fault-classification methods.

Index Terms— Condition monitoring, fault classification, GTKWave, Icarus Verilog, industrial motor, rule-based classification, VCD, Verilog HDL.

I. INTRODUCTION

Induction motors are widely used in industrial applications owing to their simple construction, reliability, and suitability for continuous operation. Motor faults can interrupt production and increase maintenance requirements, making condition monitoring and early fault diagnosis important for reliable operation. Common faults include bearing faults, rotor faults, stator faults, and other electrical or mechanical abnormalities. Consequently, various condition-monitoring methods have been investigated to identify changes in motor behavior before they develop into severe failures [1], [2].

Several electrical and mechanical signals can be used for motor fault diagnosis. Motor current signature analysis is a widely studied approach because current can be monitored without direct interference with machine operation. Previous studies have investigated motor-current signals in different analysis domains for identifying electrical and mechanical faults [1]. Multi-signal approaches have also been explored to improve fault discrimination. For example, an ensemble-based method combined vibration and stator-current signals, extracted frequency-related features, and used multiple Random Forest classifiers for fault diagnosis [3]. Such approaches demonstrate the usefulness of signal processing and data-driven classification while generally relying on measured motor data and associated feature-extraction procedures.

Hardware-oriented approaches have also been investigated for motor condition monitoring. FPGA-based systems have been developed for signal acquisition and processing, including approaches involving Hilbert-transform-based analysis of induction-motor signals [4]. These studies demonstrate the potential of dedicated hardware for motor monitoring and diagnosis. However, advanced diagnostic approaches may require specialized signal processing, training data, or dedicated hardware platforms. A simulation-based HDL approach can therefore provide an intermediate design stage in which the behavior of a fault-classification architecture can be evaluated before physical implementation.

This work presents a Verilog HDL-based simulation framework for multi-parameter industrial motor fault classification. The framework models motor current, vibration, temperature, rotor flux, stator flux, and supply voltage as simulated motor-condition parameters. These parameters are evaluated using deterministic decision logic to classify predefined operating and fault conditions and generate a compact 3-bit fault code. The design is organized as a modular HDL system and simulated using Icarus Verilog, with generated Value Change Dump (VCD) files examined through GTKWave.

The main contribution of this work is a lightweight hardware-oriented simulation framework that combines multi-parameter motor-condition modeling, deterministic fault classification, compact fault encoding, and waveform-level verification within a Verilog-based design flow. The present work is limited to simulation and does not include physical motor measurements or FPGA implementation. Hardware deployment and experimental validation are considered possible directions for future work.

II. RELATED WORK

Research on induction-motor fault diagnosis includes signal-based condition monitoring, machine-learning classification, and hardware-oriented implementations. These approaches use different combinations of electrical and mechanical measurements, signal-processing techniques, and classification methods.

A. Signal-Based Fault Diagnosis

Induction-motor condition monitoring commonly uses parameters such as stator current, vibration, voltage, and

temperature. Gundewar and Kane reviewed several monitoring techniques and discussed the usefulness of vibration- and motor-current-based approaches for identifying mechanical and electrical abnormalities [2].

Yang et al. investigated fault diagnosis using vibration and stator-current signals. Frequency-related features were extracted from the signals and classified using an ensemble of Random Forest classifiers with weighted decision making [3]. Such approaches demonstrate the value of combining information from multiple motor signals, although they generally depend on measured data and additional signal-processing stages.

B. Machine-Learning-Based Classification

Machine-learning techniques have also been applied to automatically distinguish different motor-fault conditions. Lee and Lin investigated induction-motor fault classification using current signals and Hilbert-Huang Transform-based feature extraction. Different feature-selection methods and classifiers, including SVM, KNN, and decision trees, were evaluated for fault classification [5].

These methods illustrate the use of feature-based classification but generally require a processing pipeline involving feature extraction, feature selection, and classification. Their implementation may therefore involve more processing stages than a deterministic rule-based approach.

C. FPGA and Hardware-Oriented Diagnosis

Hardware-based motor monitoring has been explored using FPGA platforms. Millan-Almaraz et al. developed an FPGA-based induction-motor monitoring system using wavelet-based signal analysis for detecting broken rotor bars [6]. Juarez-Trujillo et al. later presented an FPGA-based fault-analysis system involving signal acquisition, Hilbert-transform processing, and spectral analysis of motor signals [4].

These studies demonstrate the use of programmable hardware for motor-fault monitoring. In contrast, the present work focuses on the simulation stage rather than physical FPGA implementation.

D. Positioning of the Present Work

The reviewed studies mainly focus on measured motor signals, advanced signal processing, machine-learning methods, or hardware implementations. The present work instead develops a Verilog HDL simulation framework in which multiple simulated motor parameters are evaluated using deterministic decision logic and mapped to compact 3-bit fault codes.

The framework therefore represents a design-stage approach between fault modeling and physical hardware implementation. Its purpose is to examine the behavior of the classification architecture through Verilog simulation and waveform analysis, while leaving physical motor testing and FPGA deployment for future work.

III. PROPOSED FRAMEWORK

The proposed system is a Verilog HDL-based simulation framework for classifying industrial motor operating and fault conditions using multiple simulated motor parameters. The framework consists of motor signal generation, feature processing, rule-based classification, and waveform-level verification. The overall processing flow is:

Motor Signal Generation → Feature Processing → Rule-Based Classifier → 3-bit Fault Code → VCD/GTKWave

The framework considers six simulated motor parameters: motor current, vibration, temperature, rotor flux, stator flux, and supply voltage. Predefined signal conditions represent different motor operating and fault states. These signals are evaluated using deterministic decision logic to generate the corresponding fault code.

A. Fault Classification

Each operating condition is represented using a 3-bit fault code, as shown in Table I.

TABLE I
FAULT CLASSIFICATION ENCODING

Motor Condition	Fault Code
Healthy	000
Rotor fault	001
Stator fault	010
Bearing fault	011
Voltage fault	100
Overload	101

The classification uses predefined parameter conditions. For example, increased current with reduced rotor flux represents a rotor fault, while increased vibration represents a bearing fault. Reduced supply voltage is used to identify a voltage fault. The classifier uses priority-based conditional logic when multiple abnormal conditions are present.

B. HDL Simulation and Verification

The framework is implemented in Verilog HDL and simulated using Icarus Verilog. A testbench controls the simulated operating conditions and generates a Value Change Dump (VCD) file containing the relevant signal transitions. GTKWave is used to examine the simulated motor parameters and corresponding fault-code output.

This approach enables the relationship between simulated motor conditions and classification outputs to be examined at the waveform level without physical motor hardware. The documented simulation sequence includes healthy, rotor, stator, bearing, and voltage-fault conditions, while the overload condition is additionally defined using fault code 101.

IV. MOTOR SIGNAL AND FAULT MODELING

The framework models motor operating conditions using six simulated parameters: motor current, vibration, temperature, rotor flux, stator flux, and supply voltage. These parameters are varied at predefined simulation intervals to represent normal and faulty operating conditions.

A. Simulated Motor Parameters

Motor current and temperature represent electrical loading and thermal behavior, while vibration represents mechanical disturbances. Rotor and stator flux represent electromagnetic conditions, and supply voltage is used to identify voltage-related abnormalities. Selected parameters are varied according to the simulated fault condition, while the remaining parameters are maintained comparatively stable where appropriate.

B. Fault Condition Modeling

The fault conditions are represented through characteristic parameter changes. A rotor fault uses increased current and reduced rotor flux, while a stator fault uses increased current and reduced stator flux. A bearing fault is represented by increased vibration, and a voltage fault by reduced supply voltage. The overload condition is defined using increased current and temperature.

TABLE II
SIMULATED FAULT CONDITIONS

Condition	Code	Principal Parameter Behavior
Healthy	000	Normal parameter ranges
Rotor fault	001	High current, reduced rotor flux
Stator fault	010	High current, reduced stator flux
Bearing fault	011	High vibration
Voltage fault	100	Reduced supply voltage
Overload	101	High current, high temperature

The documented live simulation provides representative parameter combinations for the first five classifications. The healthy case uses 50 A current, a vibration value of 20, a

temperature of 40, rotor and stator flux values of 100, and a supply voltage of 230 V. The subsequent rotor, stator, bearing, and voltage cases modify the relevant parameters and produce codes 001, 010, 011, and 100, respectively.

The overload state (101) is defined in the classification architecture and project documentation but is not included as an independently demonstrated state in the documented live simulation sequence. Therefore, it is treated as a defined fault condition rather than a separately verified simulation result.

V. VERILOG IMPLEMENTATION AND SIMULATION VERIFICATION

The proposed framework is implemented in Verilog HDL using a modular structure comprising the motor-signal generator, feature-processing logic, fault classifier, and testbench. The signal generator produces predefined motor-condition values, while the classification logic evaluates the simulated conditions and generates the corresponding 3-bit fault code. The testbench controls the simulation and records signal transitions for waveform analysis.

The design was compiled and simulated using Icarus Verilog. During simulation, the testbench generates a Value Change Dump (VCD) file containing the relevant signal transitions. The VCD file is examined using GTKWave to observe the relationship between the simulated motor parameters and the fault-classification output. The simulation flow is:

Verilog Source Files → Icarus Verilog → VCD Generation → GTKWave

The documented simulation sequence produces fault codes 000, 001, 010, 011, and 100, corresponding to healthy, rotor, stator, bearing, and voltage-fault conditions, respectively. The overload code 101 is defined in the classification scheme but is not included in the documented live simulation sequence. Therefore, it is treated as a defined condition rather than a separately demonstrated simulation result.

The verification is limited to HDL simulation and waveform analysis. No physical motor, sensor-acquisition system, or FPGA hardware is used in the reported implementation. Thus, the results demonstrate the behavior of the simulated classification logic under the predefined test conditions rather than experimental motor-fault detection performance.

VI. RESULTS

The Verilog framework was simulated using the predefined motor operating and fault conditions described in Section IV. The resulting signal transitions were examined using GTKWave, and the resulting 3-bit fault codes were examined against the corresponding predefined classification states.

A. Simulation Results

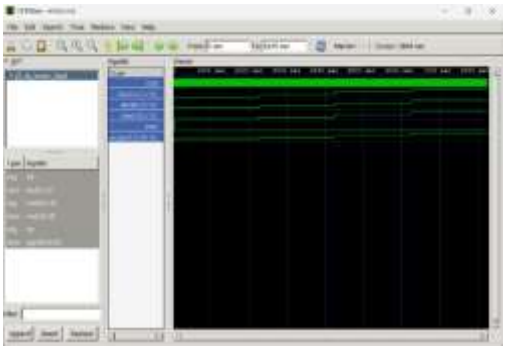
The documented simulation directly demonstrates five operating conditions. The corresponding results are summarized in Table III.

TABLE III
DOCUMENTED SIMULATION RESULTS

Test Condition	Representative Parameter Change	Fault Code	Classification
Normal operation	Parameters within normal range	000	Healthy
Rotor fault	Increased current, reduced rotor flux	001	Rotor fault
Stator fault	Increased current, reduced stator flux	010	Stator fault
Bearing fault	Increased vibration	011	Bearing fault
Voltage fault	Reduced supply voltage	100	Voltage fault

The documented simulation begins with normal operation (000), followed by rotor, stator, bearing, and voltage-fault conditions represented by 001, 010, 011, and 100, respectively. The corresponding parameter changes are observed in the simulation waveforms.

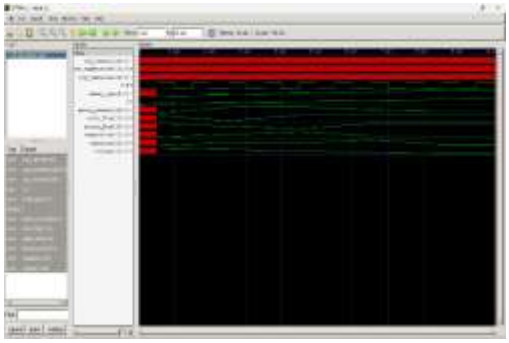
Fig. 1. Overall GTKWave waveform showing simulated motor parameters and the corresponding fault-classification output.



B. Waveform Verification

The GTKWave waveform provides signal-level observation of the simulated motor parameters and classification output. The waveform allows changes in motor current, vibration, temperature, rotor flux, stator flux, voltage, and fault_type[2:0] to be examined together and correlated with the simulated operating conditions.

Fig. 2. Extended GTKWave waveform showing fault, mode, RMS, reset, and signal transitions during simulation.



C. VCD-Based Signal Observation

The simulation generates a Value Change Dump (VCD) file containing digital signal transitions. The VCD waveform provides an additional view of the HDL simulation and allows individual signal changes to be inspected.

Fig. 3. Raw VCD waveform showing digital signal transitions during simulation.



D. Simulation Output

The directly documented classification sequence is:

000 → 001 → 010 → 011 → 100

corresponding to:

Healthy → Rotor → Stator → Bearing → Voltage fault.

The overload condition (101) is defined in the classification architecture but is not included in the directly documented live simulation sequence. Therefore, it is not counted as an independently demonstrated result in this section.

VII. LIMITATIONS AND FUTURE WORK

The present work is limited to Verilog HDL simulation and does not include measurements from a physical motor or a sensor-acquisition interface. Motor current, vibration, temperature, rotor flux, stator flux, and supply voltage are represented using predefined simulated conditions. Therefore, the reported results demonstrate the functional behavior of the

classification logic under the specified simulation conditions rather than its performance under real motor operating conditions.

The classification method uses deterministic rules and predefined fault conditions. Although this provides a simple and traceable decision process at the waveform level, it does not account for practical factors such as sensor noise, measurement uncertainty, varying motor loads, transient operating conditions, or complex combinations of simultaneous faults. The present framework also does not evaluate classification accuracy using measured fault data. In addition, the overload code 101 is defined in the classification architecture but is not included in the directly documented live simulation sequence.

Future work can incorporate measured motor signals and more realistic variations into the simulation environment. Noise, changing load conditions, transient behavior, and additional fault cases can be introduced to evaluate the classification logic under a wider range of operating conditions. The fault models can also be extended to represent multiple simultaneous abnormalities and more varied parameter combinations.

The Verilog design can subsequently be synthesized and implemented on an FPGA with suitable sensor interfaces for hardware-level testing. Such an implementation would allow the simulated classification architecture to be evaluated using actual motor-condition signals. Further work can also investigate more advanced feature-processing techniques and machine-learning-based classification methods as alternatives or extensions to the current deterministic rule-based approach.

VIII. CONCLUSION

This work presented a Verilog HDL-based simulation framework for multi-parameter industrial motor fault classification. The framework models motor operating conditions using simulated motor current, vibration, temperature, rotor flux, stator flux, and supply voltage. These parameters are evaluated using deterministic decision rules to generate a compact 3-bit fault code representing predefined motor operating and fault conditions.

The proposed design was organized as a modular HDL system comprising motor signal generation, feature processing, classification logic, and a simulation testbench. The design was compiled and simulated using Icarus Verilog, while Value Change Dump (VCD) generation and GTKWave were used for waveform-level observation. The documented simulation demonstrated the classification of healthy, rotor, stator, bearing, and voltage-fault conditions using the corresponding fault codes 000, 001, 010, 011, and 100. The overload condition was also defined in the classification architecture using code 101, although it was not included in the directly documented live simulation sequence.

The simulation results provide a waveform-level view of the relationship between the predefined motor parameters and the classification output. These results demonstrate the functional behavior of the classification logic under the specified simulation conditions and provide a basis for further development toward physical implementation.

The present work is limited to HDL simulation and does not include validation using a physical motor, sensor-acquisition system, or FPGA platform. Consequently, the results represent simulation-level functional verification rather than experimental motor-fault detection performance. Future development can incorporate measured sensor inputs, noise, varying load conditions, transient behavior, additional fault combinations, and FPGA implementation. More advanced feature-processing and machine-learning-based classification methods can also be investigated as extensions to the present deterministic approach.

REFERENCES

[1] P. Gangsar and R. Tiwari, “Signal based condition monitoring techniques for fault detection and diagnosis of induction motors: A state-of-the-art review,” *Mechanical Systems and Signal Processing*, vol. 144, Art. no. 106908, 2020, doi: 10.1016/j.ymssp.2020.106908.

[2] S. K. Gundewar and P. V. Kane, “Condition monitoring and fault diagnosis of induction motor,” *Journal of Vibration Engineering & Technologies*, vol. 9, pp. 643–674, 2021, doi: 10.1007/s42417-020-00253-y.

[3] X. Yang, R. Yan, and R. X. Gao, “Induction motor fault diagnosis based on ensemble classifiers,” in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (I2MTC)*, 2016, doi: 10.1109/I2MTC.2016.7520470.

[4] I. A. Juarez-Trujillo, S. De León Aldaco, J. G. Velásquez-Aguilar, and J. Aguayo-Alquicira, “Fault analysis in induction motors through signal acquisition with Hilbert transform and FPGA,” *IEEE Embedded Systems Letters*, vol. 17, no. 6, pp. 390–393, 2025, doi: 10.1109/LES.2025.3546847.

[5] C.-Y. Lee and W.-C. Lin, “Induction motor fault classification based on ROC curve and t-SNE,” *IEEE Access*, vol. 9, pp. 56330–56343, 2021, doi: 10.1109/ACCESS.2021.3072646.

[6] J. R. Millan-Almaraz, R. D. J. Romero-Troncoso, L. M. Contreras-Medina, and A. Garcia-Perez, “Embedded FPGA based induction motor monitoring system with speed drive fed using multiple wavelet analysis,” in *Proc. IEEE 3rd Int. Symp. Industrial Embedded Systems (SIES)*, 2008, doi: 10.1109/SIES.2008.4577702.