

# DESIGN AND IMPLEMENTATION OF SATURATION-BASED IMAGE DEHAZING ALGORITHM

M. Bharath Kumar <sup>1</sup>, Dr. G. Appala Naidu <sup>2</sup>

<sup>1</sup>Post Graduate student, ECE Department, JNTIGV-CEV

[mattabharathkumar2002@gmail.com](mailto:mattabharathkumar2002@gmail.com)

<sup>2</sup>Associate Professor, ECE Department, JNTIGV-CEV

[Ganaidu.ece@jntugvce.edu.in](mailto:Ganaidu.ece@jntugvce.edu.in)

**Abstract:** Atmospheric haze significantly degrades image quality by causing light scattering, which leads to reduced contrast, color distortion, and loss of visual details. To address these challenges, this work presents a hardware-efficient image dehazing system based on an optimized VLSI architecture that combines the Dark Channel Prior (DCP) method with a saturation-based transmission estimation approach. The proposed design utilizes a 5×5 minimum filter applied to a down sampled image for accurate atmospheric light estimation while substantially reducing computational complexity and hardware overhead. Furthermore, a saturation-guided pixel-level transmission model is employed to effectively mitigate halo artifacts and preserve fine image structures during restoration. The dehazing algorithm is initially validated using MATLAB simulations and subsequently implemented in Verilog HDL on a Zynq-7000 FPGA platform. Experimental results demonstrate that the proposed architecture achieves improved image restoration performance in terms of Peak Signal-to-Noise Ratio (PSNR) and Structural Similarity Index Measure (SSIM), while requiring lower logic resources and reduced power consumption compared to existing implementations. The proposed solution offers an effective trade-off between dehazing quality and hardware efficiency, making it highly suitable for real-time embedded vision applications, including intelligent surveillance, autonomous navigation systems, and outdoor imaging in challenging weather conditions.

**Keywords:** Image Dehazing, FPGA, Dark Channel Prior, Saturation Mapping, VLSI Architecture, Real-Time Processing.

## 1. INTRODUCTION

Atmospheric conditions such as haze and fog cause significant light scattering, leading to substantial degradation in outdoor image quality. This degradation is characterized by reduced contrast, color distortion, and the loss of important scene details, which adversely affects image visibility and interpretation. Consequently, the performance of vision-based systems is compromised, particularly in applications such as intelligent transportation, surveillance, and environmental monitoring, where accurate real-time image analysis is essential for reliable operation and decision-making.

To mitigate these effects, image dehazing techniques are employed to restore visibility by compensating for atmospheric scattering. However, conventional software-based approaches often rely on computationally intensive algorithms or deep learning models that demand substantial processing power and memory resources, making them unsuitable for resource-constrained embedded systems. Although hardware-based implementations can provide the high processing speed required for real-time applications, they frequently face challenges in maintaining restoration quality while adhering to strict constraints on power

consumption, hardware complexity, and computational resources.

A key challenge in hardware-based image dehazing is the efficient estimation of atmospheric light and transmission maps. Conventional methods often suffer from

oversaturation, loss of detail, and halo artifacts. To overcome these limitations, the proposed approach employs a 5×5 minimum filter on down sampled images for accurate atmospheric light estimation and a pixel-level transmission model that preserves image textures. Based on an enhanced Dark Channel Prior, the FPGA implementation achieves real-time dehazing with improved visual quality, higher restoration performance, and efficient hardware utilization, making it well suited for embedded vision applications.

## 2. LITERATURE REVIEW

Early image dehazing techniques primarily relied on prior-based methods that exploit statistical characteristics of haze-free images. Among these, the Dark Channel Prior (DCP) proposed by He et al. [2] became widely adopted due to its effectiveness in estimating scene transmission. However, conventional

DCP suffers from halo artifacts around depth discontinuities and requires large minimum-filter windows, increasing computational complexity. Subsequent improvements using guided and joint bilateral filters enhanced transmission estimation but introduced additional processing overhead [7], [8]. Other approaches, such as color attenuation priors [5] and structure-preserving priors [6], improved image contrast and depth perception but remained computationally intensive. To address these limitations, saturation-based transmission estimation methods were introduced. Kimetal. [3] proposed a pixel-level saturation-driven approach that eliminates patch-based averaging and reduces halo artifacts while improving computational efficiency, making it well suited for real-time hardware implementation.

Beyond prior-based techniques, methods such as linear transformation [9] and multi-exposure image fusion [10] were developed to reduce computational complexity. While these approaches offer faster processing, they often struggle with detail preservation and edge handling. Deep learning models, including Dehaze Net [11] and AOD-Net [12], provide superior restoration quality but require substantial computational and memory resources, limiting their use in FPGA and ASIC implementations. In hardware-based dehazing, a key challenge is balancing filter size, image quality, and resource utilization. To address this, Upadhyay and Sarawadekar [1] proposed a saturation-based VLSI architecture with optimized filtering, enabling real-time dehazing with improved hardware efficiency.

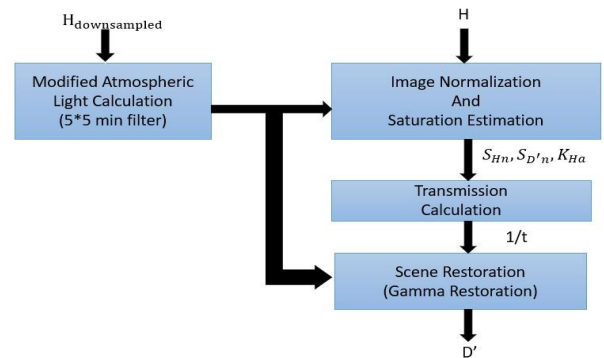
Despite significant advancements, there remains a need for a dehazing architecture that balances image quality and hardware efficiency. To address this gap, the present work employs a  $5 \times 5$  minimum filter on down sampled images along with saturation - based transmission estimation, and implements the design in MATLAB and Verilog for FPGA deployment. The proposed approach improves atmospheric light estimation while reducing hardware complexity, offering an effective compromise between the limitations of small- and large-window filter designs.

### 3. METHODOLOGY

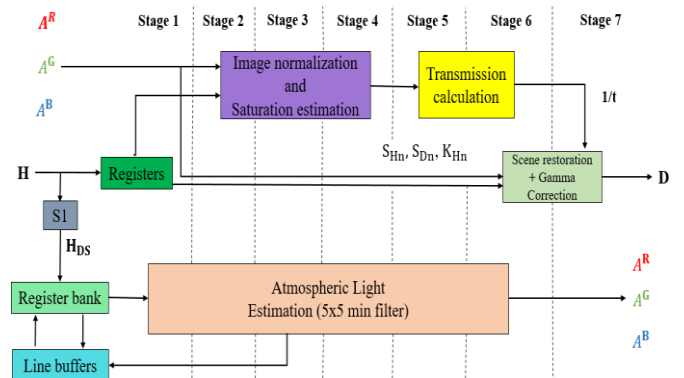
As illustrated in Fig.1, the proposed image dehazing framework consists of a sequence of hardware-efficient processing stages. Initially, a coarse dark-channel map is generated from a  $2\times$  down sampled input image by applying a  $5\times 5$  minimum filter to the minimum values of the RGB channels. This reduced-resolution dark channel is used to estimate the atmospheric light with lower computational complexity. Simultaneously, the full-resolution image is normalized using the estimated atmospheric light, and a pixel-level saturation map is computed to characterize local haze conditions. The transmission map is then estimated from the normalized dark-channel values and refined using saturation-based weighting to preserve image details. To

ensure numerical stability, the transmission values are constrained to a predefined minimum threshold. Finally, the haze-free image is reconstructed by compensating for atmospheric scattering through transmission-guided restoration, followed by gamma correction using a lookup table (LUT) to enhance brightness, contrast, and overall visual quality.

The proposed methodology enhances existing saturation-based VLSI dehazing techniques by incorporating the Dark Channel Prior (DCP) with hardware-oriented algorithmic optimizations. The algorithm is first developed and validated using a floating-point MATLAB reference model, followed by its implementation in fixed-point Verilog HDL for FPGA prototyping. The complete design flow is illustrated in Fig. 2, and the individual processing stages are described in the following subsections.



**Figure 1:** Flow Diagram of implemented dehazing algorithm



**Figure 2:** Block diagram of the proposed VLSI architecture for dehazing.

### 3.1 Input Acquisition and Pre-Processing

The input hazy image is acquired in RGB format and normalized to the range  $([0,1])$  in MATLAB. For hardware implementation, pixel values are represented using a 12-bit fixed-point (Q0.12) format to reduce computational complexity and memory usage while maintaining adequate precision. To further improve hardware efficiency, the image is down sampled by a factor of two using bilinear interpolation, and the resulting reduced-resolution image is

utilized for dark-channel computation and atmospheric light estimation.

$$H(x) = D(x)t(x) + A(1 - t(x)) \quad (1)$$

### 3.2 Dark Channel Computation

Let  $I_c(x)$  denote the intensity of channel  $c \in \{R, G, B\}$  at pixel  $x$ , and let  $\Omega(x)$  be a  $5 \times 5$  neighborhood centered at  $x$ . The dark channel is computed as:

$$I^{dark}(x) = \min_{c \in \{R, G, B\}} \left( \min_{y \in \Omega(x)} I_c(y) \right) \quad (2)$$

The two-stage minimum operation provides a reliable estimate of the locally darkest intensity within each image patch. To reduce computational complexity and hardware resource utilization, this operation is performed on the down sampled image.

### 3.3 Atmospheric Light Estimation (ALE)

The atmospheric light is estimated by identifying the brightest 0.1% of pixels in the dark channel and selecting the corresponding pixel in the original full-resolution image with the highest combined RGB intensity. This strategy provides a reliable estimate of the global atmospheric light.

$$A = [A_R, A_G, A_B] = \arg \max_{x \in P} \sum_{c \in \{R, G, B\}} H_c(x) \quad (3)$$

Here,  $P$  denotes the set of the top 0.1% brightest pixels in the dark channel. To improve hardware efficiency, percentile selection is implemented using a streaming histogram with cumulative counting, eliminating the need for full sorting and significantly reducing memory and comparator requirements.

### 3.4 Saturation-Based Transmission Estimation

Each pixel is normalized by the atmospheric light:

$$H_c(x) = \frac{I_c(x)}{A_c} \quad (4)$$

and the saturation  $S(x)$  is computed from the normalized channels as:

$$S_H(x) = 1 - \frac{\min(H_R, H_G, H_B)}{\frac{H_R + H_G + H_B}{3}} \quad (5)$$

A contrast-stretch enhancement transforms  $S(x)$  to:

$$S'_H(x) = S_H(x) \cdot (2 - S_H(x)) \quad (6)$$

The transmission estimate is then:

$$t(x) = \max(1 - \psi \cdot S'_H(x), t_0) \quad (7)$$

where  $\psi = 1.25$  and  $t_0 = 0.1$ . This per-pixel formulation is inherently parallel and well suited for pipeline implementation.

### 3.5 Transmission Up Sampling

The down sampled transmission map is up sampled to full resolution using bilinear interpolation. To improve hardware efficiency, the FPGA implementation employs shift-add operations and integer arithmetic, reducing resource utilization while preserving reconstruction quality.

### 3.6 Scene Radiance Recovery

Using the atmospheric scattering model  $H(x) = D(x)t(x) + A(1 - t(x))$ , the scene radiance  $D(x)$  is recovered as:

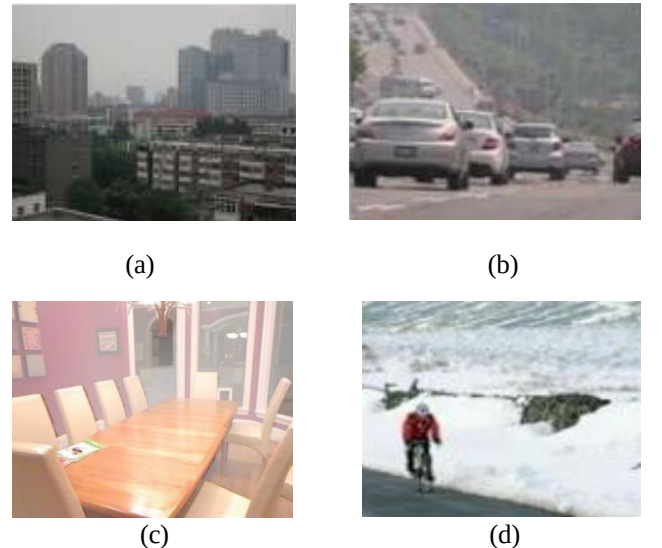
$$D(x) = \frac{H(x) - A}{\max(t(x), t_0)} + A \quad (8)$$

Finally, a gamma correction LUT is applied to improve image brightness and contrast with minimal processing latency.

## 4. RESULTS AND DISCUSSIONS

The proposed dehazing methodology was validated using two complementary platforms: MATLAB for algorithm-level simulation and Verilog HDL for FPGA-based hardware implementation. This dual-platform evaluation establishes the correlation between algorithmic performance and hardware efficiency. Comparative analysis with the baseline saturation-based VLSI dehazing architecture is presented to highlight the improvements, performance trade-offs, and hardware resource utilization of the proposed design.

The proposed method was evaluated using a diverse dataset of ten representative test images covering various real-world scenarios, including outdoor streets, indoor environments, natural landscapes, and architectural scenes. The dataset encompasses different haze conditions, ranging from mild to dense atmospheric degradation, to assess the robustness and adaptability of the proposed algorithm. By including both urban and rural scenes, the evaluation reflects practical deployment conditions for a wide range of embedded vision applications, as shown in Fig. 3.





(e)



(f)



(g)



(h)



(i)



(j)

**Figure 3:** Test images used for quantitative performance evaluation. (a) Image 1. (b) Image 2. (c) Image 3. (d) Image 4. (e) Image 5. (f) Image 6. (g) Image 7. (h) Image 8. (i) Image 9. (j) Image 10.



(a)

(b)

**Figure 4:** Simulation outcomes showcasing image restoration using the proposed Dark Channel Prior (DCP)-based dehazing technique. (a) Input hazy images and (b) Corresponding dehazed results obtained from the implemented method.

Fig. 4 illustrates the performance of the proposed Dark Channel Prior (DCP)-based dehazing method through visual comparisons of ten representative test images. The proposed approach effectively removes atmospheric haze from diverse scenes, including urban, indoor, and natural environments, resulting in improved image contrast, color fidelity, and

visibility while preserving fine structural details. The use of hardware-efficient reciprocal and gamma correction lookup tables (LUTs) enables real-time implementation with low computational complexity. These results demonstrate the robustness and effectiveness of the proposed method under varying atmospheric conditions.

#### 4.1 Verilog Implementation

The proposed hardware architecture was synthesized on the Zynq-7000 FPGA platform (XC7Z020-CLG484-1) using a seven-stage pipelined design comprising input acquisition, image down sampling, dark-channel computation, atmospheric light estimation, saturation-based transmission estimation, radiance recovery, and output generation. The architecture is optimized for real-time image dehazing while maintaining an effective balance between restoration quality, hardware resource utilization, and processing efficiency.

TABLE II  
PERFORMANCE COMPARISON OF VARIOUS  
DEHAZING METHODS

| Dataset        | VLSI architectures |        |       |        |       |        |       |        |       |        |                 |               |
|----------------|--------------------|--------|-------|--------|-------|--------|-------|--------|-------|--------|-----------------|---------------|
|                | [12]               |        | [13]  |        | [14]  |        | [15]  |        | [1]   |        | Proposed Method |               |
|                | PSNR               | SSIM   | PSNR  | SSIM   | PSNR  | SSIM   | PSNR  | SSIM   | PSNR  | SSIM   | PSNR            | SSIM          |
| SOTS (Outdoor) | 18.83              | 0.8120 | 18.29 | 0.8241 | 15.23 | 0.6562 | 15.53 | 0.6459 | 21.42 | 0.8791 | <b>23.83</b>    | <b>0.9434</b> |
| SOTS (Indoor)  | 18.42              | 0.7933 | 16.33 | 0.7697 | 16.30 | 0.7496 | 17.09 | 0.7704 | 18.68 | 0.8310 | <b>22.20</b>    | <b>0.8723</b> |
| NYU            | 11.41              | 0.6723 | 11.10 | 0.6512 | 10.86 | 0.6422 | 11.85 | 0.6889 | 12.71 | 0.7356 | <b>12.65</b>    | <b>0.7423</b> |
| O-HAZE         | 14.37              | 0.3502 | 15.60 | 0.4233 | 13.85 | 0.4565 | 13.73 | 0.3292 | 16.45 | 0.4411 | <b>18.48</b>    | <b>0.8259</b> |

Table II presents a performance comparison of the proposed architecture with existing VLSI image dehazing designs using standard benchmark datasets. The reference design in [1] employs a Dark Channel Prior (DCP) implemented through a  $15 \times 15$  minimum filter realized as a cascade of  $3 \times 3$  filters. In contrast, the proposed architecture utilizes a compact  $5 \times 5$  minimum filter together with a gamma correction stage. This modification significantly reduces memory requirements and computational complexity, resulting in lower LUT and register utilization while maintaining competitive PSNR and SSIM performance.

#### 4.2 FPGA Implementation

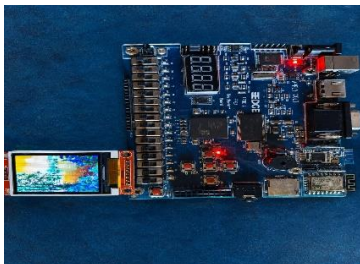


Figure 5: FPGA-based hardware implementation



Figure 6: FPGA-based hardware implementation

TABLE III  
FPGA IMPLEMENTATION RESULTS

| Architecture            | [13]         | [14]         | [16]         | [1]             | Proposed Method |
|-------------------------|--------------|--------------|--------------|-----------------|-----------------|
| Family                  | Stratix      | Stratix      | Stratix      | Zynq7000        | Zynq7000        |
| Device                  | EP1S10F780C6 | EP1S10F780C6 | EP1S10F780C6 | XC7Z020CLG484-1 | XC7Z020CLG484-1 |
| No. of LE's             | 1607         | 1094         | 3169         | 1537            | 1388            |
| Registers               | 454          | 539          | 651          | 547             | 109             |
| Frequency (MHz)         | 58.43        | 116          | 58.2         | 85.2            | 85.2            |
| Throughput (M pixels/s) | 58.43        | 116          | 58.2         | 85.2            | 85.2            |
| Power                   | -            | -            | -            | -               | 0.107w          |

Table III presents the FPGA implementation results of the proposed architecture in comparison with existing designs. The proposed implementation on the Zynq-7000 FPGA demonstrates efficient hardware utilization, requiring only 2.49% of Slice LUTs, 3.68% of LUTRAM, and 0.10% of Slice Registers. The measured on-chip power consumption is approximately 0.108 W, indicating a low-power design suitable for embedded real-time image processing. These results demonstrate that the proposed architecture achieves an effective balance between hardware efficiency and dehazing performance.

## 5. CONCLUSION

This work presents a hardware-efficient VLSI implementation of an image dehazing algorithm that integrates the Dark Channel Prior (DCP) with saturation-based transmission estimation for FPGA deployment. By employing a  $5 \times 5$  minimum filter on a down sampled image, the proposed architecture achieves accurate atmospheric light estimation while reducing computational complexity and hardware resource utilization. Experimental results demonstrate that the design provides an effective balance between image restoration quality and hardware efficiency, making it well suited for real-time embedded vision applications.

MATLAB-based validation and Verilog HDL implementation on the Zynq-7000 FPGA demonstrate that

the proposed architecture achieves improved image restoration performance in terms of PSNR and SSIM while reducing hardware resource utilization compared to existing VLSI dehazing designs. The optimized processing pipeline and compact 5×5 filter enhance both visual quality and computational efficiency. Furthermore, the FPGA implementation exhibits low power consumption and efficient logic utilization, making the proposed architecture well suited for real-time, low-power embedded vision applications.

In conclusion, the proposed work effectively bridges the gap between image restoration performance and hardware efficiency in FPGA-based dehazing systems. The integration of Dark Channel Prior (DCP) and saturation-based transmission estimation enables robust haze removal while preserving fine image details. Future work will focus on adaptive filter window selection, hardware-efficient image enhancement techniques, and high-level synthesis optimizations to further improve scalability and performance for real-time vision applications, including autonomous navigation, intelligent surveillance, and remote sensing.

## 6. FUTURE SCOPE

The proposed image dehazing system can be further enhanced by supporting high-resolution image and video processing for advanced real-time applications. Future work may integrate lightweight deep-learning techniques to improve dehazing accuracy under varying weather conditions. The architecture can also be extended to handle rain, fog, and low-light environments within a unified framework. Additionally, ASIC implementation and hardware optimization can further reduce power consumption and increase processing speed for embedded vision systems.

## References

- [1] U.-Bharat Bhushan, S.-Kishor, "VLSI Design of Saturation-Based Image Dehazing Algorithm" *IEEE Trans. on Very Large-Scale Integration (VLSI) Sys.*, vol. 31, no. 7, July 2023.
- [2] K. He, J. Sun, and X. Tang, "Single image haze removal using dark channel prior," *IEEE Trans. Pattern Anal. Mach. Intell.*, vol. 33, no. 12, pp. 2341–2353, Dec. 2011.
- [3] S. E. Kim, T. H. Park, and I. K. Eom, "Fast single image dehazing using saturation-based transmission map estimation," *IEEE Trans. Image Process.*, vol. 29, pp. 1985–1998, 2020.
- [4] B. B. Upadhyay and K. Sarawadekar, "VLSI design of saturation-based image dehazing algorithm," *IEEE Trans. VLSI Syst.*, vol. 31, no. 7, pp. 959–972, Jul. 2023.
- [5] Q. Zhu, J. Mai, and L. Shao, "A fast single image haze removal algorithm using color attenuation prior," *IEEE Trans. Image Process.*, vol. 24, no. 11, pp. 3522–3533, Nov. 2015.
- [6] L. He, J. Zhao, N. Zheng, and D. Bi, "Haze removal using the difference-structure-preservation prior," *IEEE Trans. Image Process.*, vol. 26, no. 3, pp. 1063–1075, Mar. 2017.
- [7] H. Xu, J. Guo, Q. Liu, and L. Ye, "Fast image dehazing using improved dark channel prior," *Proc. IEEE Int. Conf. Inf. Sci. Technol.*, pp. 663–667, 2012.
- [8] C. Xiao and J. Gan, "Fast image dehazing using guided joint bilateral filter," *Vis. Compute.*, vol. 28, nos. 6–8, pp. 713–721, Jun. 2012.
- [9] W. Wang, X. Yuan, X. Wu, and Y. Liu, "Fast image dehazing method based on linear transformation," *IEEE Trans. Multimedia*, vol. 19, no. 6, pp. 1142–1155, Jan. 2017.
- [10] A. Galdran, "Image dehazing by artificial multiple-exposure image fusion," *Signal Process.*, vol. 149, pp. 135–147, Aug. 2018.
- [11] B. Cai, X. Xu, K. Jia, C. Qing, and D. Tao, "Dehaze Net: An end-to-end system for single image haze removal," *IEEE Trans. Image Process.*, vol. 25, no. 11, pp. 5187–5198, Nov. 2016.
- [12] B. Li, X. Peng, Z. Wang, J. Xu, and D. Feng, "AOD-Net: All-in-one dehazing network," *Proc. IEEE Int. Conf. Compute. Vis. (ICCV)*, pp. 4780–4788, Oct. 2017.
- [13] Y. H. Shiau, H. Y. Yang, P. Y. Chen, and Y. Z. Chuang, "Hardware implementation of a fast and efficient haze removal method," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 23, no. 8, pp. 1369–1374, Aug. 2013.
- [14] B. Zhang and J. Zhao, "Hardware implementation for real-time haze removal," *IEEE Trans. Very Large-Scale Integer. (VLSI) Syst.*, vol. 25, no. 3, pp. 1188–1192, Mar. 2017.
- [15] Y.-H. Shiau, Y.-T. Kuo, P.-Y. Chen, and F.-Y. Hsu, "VLSI design of an efficient flicker-free video defogging method for real-time applications," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 29, no. 1, pp. 238–251, Jan. 2019.
- [16] Y.-T. Kuo, W.-T. Chen, P.-Y. Chen, and C.-H. Li, "VLSI implementation for an adaptive haze removal method," *IEEE Access*, vol. 7, pp. 173977–173988, 2019.