

DESIGN AND IMPLEMENTATION OF A HIGH-SPEED DUAL-MODE SCHMITT TRIGGER WITH ADAPTIVE HYSTERESIS AND ENHANCED TRANSIENT ROBUSTNESS

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Abstract- Schmitt Trigger circuits are widely used in CMOS VLSI systems to improve noise immunity and provide reliable signal transitions. However, conventional Dual-Mode Schmitt Trigger (DST) designs often exhibit limited hysteresis characteristics and reduced tolerance to transient disturbances, which can affect switching stability in high-speed digital applications. This paper presents the design and implementation of an adaptive hysteresis-based Dual-Mode Schmitt Trigger incorporating an adaptive feedback network and a power-gating transistor to enhance switching performance and transient robustness. The proposed circuit was designed and simulated using Cadence Virtuoso in 90 nm CMOS technology with a 1.2 V supply voltage. DC, transient, and Single Event Transient (SET) analyses were performed to evaluate its performance. Simulation results show that the proposed design increases the hysteresis width from 194.63 mV to 317.76 mV, resulting in improved noise immunity and stable switching characteristics. The circuit also demonstrates reliable recovery under SET current injection while maintaining high-speed operation. These improvements make the proposed architecture suitable for low-power and noise-sensitive CMOS VLSI applications.

KeyWords: Dual-Mode Schmitt Trigger, Adaptive Hysteresis, CMOS, Cadence Virtuoso, Single Event Transient, Noise Immunity, Power Gating, VLSI.

I. INTRODUCTION

Rapid advances in Very Large-Scale Integration (VLSI) technologies have resulted in a high demand for fast, power-efficient, and reliable digital circuits. Modern electronic devices including communication devices, embedded systems, automotive electronics, medical devices, Internet of Things (IoT) devices, etc., require circuits, which will be capable to operate efficiently at any working condition. With further scaling of the CMOS technology, digital circuits become more sensitive to such effects as noise, process variation, supply voltage fluctuation, and transients leading to the necessity to develop circuits with reliable signal processing.

Schmitt Trigger (ST) is a regenerative comparator circuit utilized to improve the performance of the signal by introducing the hysteresis to the input-output transfer characteristics. In contrast to a standard CMOS inverter, a Schmitt Trigger uses two different threshold voltages for rising and falling input signal. The use of hysteresis allows increasing noise immunity by excluding the switching due to slowly changing or noisy inputs. Due to the above-mentioned advantages, Schmitt Trigger circuits are extensively used in waveform shaping, signal conditioning, debounce circuits, sensors interface, oscillators, digital communications, and many other applications.

In order to increase flexibility and power efficiency, researchers have developed Dual-Mode Schmitt Triggers (DST) capable to operate in various modes depending on the application requirements. Dual-Mode Schmitt Triggers combine high speed with good power efficiency. However, conventional Dual-Mode ST architectures face certain drawbacks such as narrow hysteresis width reducing the noise immunity and transient disturbances induced by supply fluctuations and switching activity reducing the switching stability. The above-mentioned limitations give motivation to develop Schmitt Trigger architectures with improved switching and higher transient resistance.

In order to resolve the mentioned problems, this work suggests developing an adaptive hysteresis-based DST circuit including an adaptive feedback network and a power gating transistor. Adaptive feedback network will enhance the positive feedback during the switching phase resulting in wider hysteresis width and increasing noise immunity. Using a power gating transistor will allow regulating the current during the operation thus providing a more stable switching. The suggested

improvements should improve overall reliability of the Dual-Mode Schmitt Trigger keeping high-speed.

The proposed circuit has been designed and simulated using Cadence Virtuoso with 90 nm CMOS technology and 1.2 V supply voltage. The circuit performance has been tested via DC analysis, transient analysis, and Single Event Transient (SET) current injection analysis. The simulation results show that the suggested circuit enlarges the hysteresis width up to 317.76 mV from 194.63 mV providing a higher noise immunity and stable switching.

II. LITERATURE SURVEY

The use of Schmitt Trigger (ST) circuits in CMOS ICs has attracted much attention due to their hysteresis properties enabling noise rejection and reliable switching. ST circuits find widespread application in applications where waveform shaping, sensor interfacing, communication systems, oscillators, and other mixed-signal circuits with reliable switching are needed in noisy environments. Due to continuous technological advances in CMOS ICs, the need for Schmitt Trigger circuits having low power consumption, fast switching speed, and high reliability has been steadily increasing [1], [2].

Many approaches aimed at improvement of ST's switching performance and noise rejection capabilities have been recently developed. Al-Sarawi [6] proposed a low-power CMOS Schmitt Trigger whose performance in terms of energy efficiency has been greatly improved. However, the proposed approach had some limitations in the sense that the hysteresis parameters were constant being set up by a static feedback network. In a similar way, Melek et al. [10] analyzed the operation of the classical CMOS Schmitt Trigger circuits working in subthreshold regime, proving their reliable operation at low voltage, however lacking adaptability.

For the sake of improvement of the circuit speed, domino logic was added to the ST architecture. Thus, Singh et al. [3] proposed Schmitt Trigger circuits working on the basis of domino logic. As a result, the authors managed to obtain circuits with good switching performance and relatively good noise rejection capability. Ramakrishna et al. [4] enhanced domino Schmitt Trigger circuits by widening the hysteresis

voltage and thus providing the increase in the stability of the switching process and decrease in propagation delay time. Nevertheless, these architectures are mostly based on regenerative feedback which does not allow to control the hysteresis window in varying operating conditions.

Furthermore, the recent researches deal with the problem of improving the reliability of the ST circuit in case of process variations and transient disturbances. The Schmitt Trigger circuit resistant to the process variation and NBTI has been proposed by Shah et al. [2]. The authors managed to create Schmitt Trigger circuit with improved stability in case of aging effects. A radiation-hardened domino logic-based Schmitt Trigger [1] has been proposed for obtaining increased noise immunity and transient robustness in nanoscale CMOS technologies. Gadlage et al. [5] studied SETs in Schmitt Trigger inverter chains working at subthreshold voltages and proved that transient disturbances might greatly affect switching process in scaled CMOS technologies. From these studies it is possible to state that more and more attention is paid to the problem of designing circuits having reliable operation in case of transient disturbances.

Moreover, DTMOS technology has been applied in order to increase the electromagnetic immunity of the circuit and switching performance. Kim and Kim [9] showed that Schmitt Trigger logic gates based on DTMOS have great robustness in case of low-voltage operation, while Fernandes et al. [8] have designed three-inverter Schmitt Trigger able to operate at very low voltages (at the level of 50 mV). Despite the fact that all these architectures greatly improve some performance parameters, there are no works combining adaptive hysteresis enhancement and transient-aware operation in Dual-Mode Schmitt Trigger configuration.

It should be noted that much progress has been made in the field of reduction of power consumption, increasing of switching speed and improvement of circuit reliability. Nevertheless, most of the ST circuits are focused on one or several aspects of improvement separately. Almost no works deal with the integration of adaptive feedback with the power-gating technique in a Dual-Mode Schmitt Trigger configuration. That is why this work aims to propose the adaptive hysteresis-based Dual-Mode Schmitt Trigger

designed in 90 nm CMOS technology. The incorporation of the adaptive feedback transistor along with the power-gating transistor enables obtaining wider hysteresis characteristics, increased switching stability and transient immunity in the proposed circuit.

III. PROPOSED METHODOLOGY

A. EXISTING DUAL-MODE SCHMITT TRIGGER

The Conventional Dual-Mode Schmitt Trigger (DST) is taken as a basis for the new proposed design. The combination of a switching function of a Schmitt Trigger and domino logic flexibility allows producing reliable output transitions of the circuit regardless of the type of the input signal. Regenerative feedback is used in order to generate hysteresis and make the circuit more immune to noise.

As it is shown in Fig. 1, the transistor-level diagram of the Conventional Dual-Mode Schmitt Trigger contains three basic blocks: the input control stage, the regenerative switching stage, and the output inverter stage. These blocks work together to provide hysteresis effect and a reliable output transition. Three types of input signals are provided to the logic block shown on the left side of Fig. 1: the input voltage V_{in} , the clock CLK, and the control signal CTRL. The generated control output controls the working of the transistor network and makes the circuit operate in one of two modes depending on the applied control signal: either in the Schmitt Trigger mode or in domino logic mode.

Regenerative switching stage contains transistors M1, M2, M3, M6, and M7. Transistors M1, M2, and M3 make up the primary switching path that is responsible for charging and discharging of the internal node V_{out1} . Depending on the applied input signal the conduction state of these transistors varies thus providing switching behavior of the circuit. Voltage at V_{out1} is the intermediate node that determines the output transition.

Transistor M6 is responsible for providing regenerative feedback necessary for generating hysteresis. In course of the switching process, the feedback path influences the effective switching threshold changing the voltage at V_{out1} . This positive feedback technique allows making two switching thresholds, one for rising input transition and one for

falling transition, thus making the circuit more immune to noise compared to the conventional CMOS inverter.

Transistor M7 is the mode-control transistor which makes the connection between control stage and the regenerative switching network. Depending on the control signal, M7 provides the required current path for the selected mode and also helps to control the regenerative feedback process. This transistor plays a vital role in the dual-mode functionality of the circuit.

Output stage includes transistors M4 and M5 that make up the CMOS inverter connected to the internal node V_{out1} . Thus, this stage restores the logic level and provides the final output V_{out2} with full voltage swing. Isolating the internal feedback node from the external load, the output inverter improves the signal integrity and provides reliable output transitions. In case of the rising transition of the input signal, regenerative feedback delays the switching action until the input voltage becomes greater than the upper threshold voltage. Likewise, in case of the falling transition, the feedback network decreases the switching threshold prior to the output state change. The difference between these two thresholds provides the hysteresis window, which excludes any additional output transitions caused by input noise and thus makes the switching more reliable.

Although the Conventional Dual-Mode Schmitt Trigger provides a reliable switching behavior and is more immune to noise than the ordinary CMOS inverter, its hysteresis properties are mainly determined by the fixed transistor configuration. Therefore, the regenerative feedback strength remains the same in the course of the operation, and the hysteresis window cannot be adjusted depending on the input signal. Moreover, this circuit demonstrates low tolerance to transient disturbances like power noise and Single Event Transients.

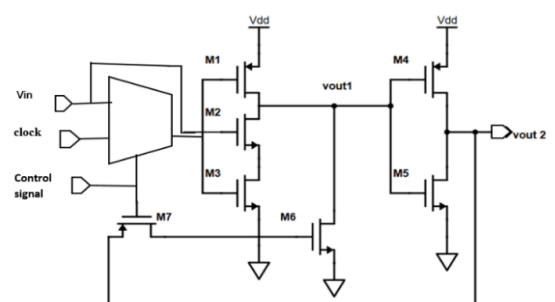


Fig 1: Conventional Dual-Mode Schmitt Trigger Architecture

B. PROPOSED DUAL-MODE SCHMITT TRIGGER

In order to deal with the mentioned shortcomings of the conventional Dual-Mode Schmitt Trigger (DST), an adaptive hysteresis architecture is presented by adding new transistors to the existing circuit structure. Thus, the presented circuit design retains the basic working principles of the conventional Dual-Mode Schmitt Trigger but includes a power-gating transistor (M1), an adaptive feedback transistor (M5) and a new output transistors group (M8, M9).

Figure 2 shows the transistor-level structure of the presented adaptive hysteresis-based Dual-Mode Schmitt Trigger. As it can be seen, the input control stage is left intact and continues receiving input signals such as V_{in} , Clock and Control, which define the mode of operation and activate the regenerative switching stage. The original switching transistors M2, M3, M4, M6 and M7 are preserved in the circuit to retain the basic functioning principle of the conventional DST.

First of all, the introduced transistor M1 connects the supply voltage (V_{DD}) to the regenerative switching stage. The transistor M1 is called power-gating transistor and it controls the current that flows from the supply voltage to the regenerative switching stage. During the operation of the circuit, the power-gating transistor M1 supplies the switching stage with a controlled current necessary for reliable switching while excluding superfluous current flow. Such controlled power supply ensures efficient operation of the circuit and helps it to remain stable in case of transient disturbance.

Second, an additional transistor M5 is introduced to the regenerative feedback path of the circuit. In the conventional DST circuit, the feedback strength is static, as it only depends on the particular transistor configuration. In the presented design, transistor M5 dynamically reinforces the regenerative feedback during switching transitions. The introduced feedback affects the charging/discharging process at the internal node (V_{out1}) leading to a higher separation between the upper and lower switching threshold. As a result, the hysteresis window of the circuit is increased, which ensures better immunity to noise and reduces the number of output transitions induced by slowly varying or noisy input signal.

Finally, to improve the performance of the switching process, transistors M8 and M9 are included in the output part

of the circuit. They help to establish an additional switching path that supports the operation of the output inverter in the process of switching. Thus, transistors M8 and M9 improve the stability of the final output (V_{out2}) and help the circuit to recover faster from transient disturbances. Moreover, their inclusion helps to retain the stable logic level under the Single Event Transient (SET) conditions due to reduction of the impact of the temporary voltage changes at the internal feedback node.

Thus, the presented circuit can be represented as a composition of three parts, namely input control stage, adaptive regenerative switching stage and output stage. The input control stage is responsible for determining the mode of operation of the circuit. The adaptive regenerative switching stage performs the generation of adaptive hysteresis due to the interaction of the adaptive feedback transistor M5 and the feedback network. Finally, the enhanced output stage composed of M6, M7, M8 and M9 restores the output logic level.

Comparing the proposed architecture with the conventional Dual-Mode Schmitt Trigger, one should note the increase of hysteresis width, higher regenerative feedback, improved current control and transient robustness. Thus, the introduced adaptive feedback transistor increases the threshold separation during switching, while the power-gating transistor helps to control the current in the circuit. Additionally, the introduction of the new transistors to the output stage leads to improved output stability and ensures reliable operation in the case of transient disturbance conditions. As it was shown during simulation, the proposed design increases the hysteresis window up to 317.76 mV compared to 194.63 mV of the conventional circuit and helps to ensure stable recovery in the case of SET current injection analysis.

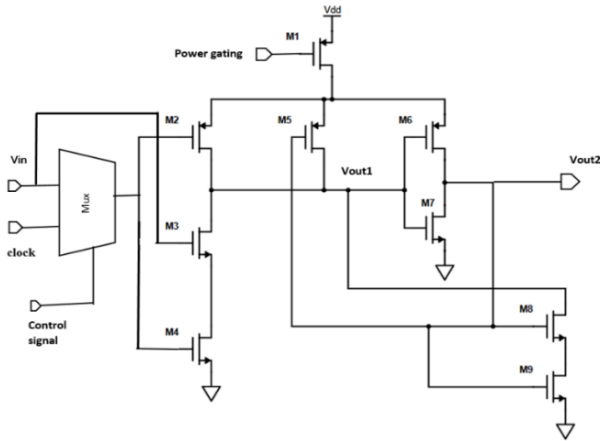


Fig 2: Proposed Dual-Mode Schmitt Trigger Architecture

C. DESIGN IMPROVEMENTS OF THE PROPOSED CIRCUIT

The architecture of the proposed Dual-Mode Schmitt Trigger is realized by adding four transistors to the conventional DST circuitry without changing the main principles of its operation. The changes implemented in the proposed architecture are aimed at enhancing such parameters of the circuit as hysteresis properties, switching stability and transient robustness. Comparing with the conventional circuitry, the architecture of the proposed DST includes power-gating transistor M1, adaptive feedback transistor M5 and two additional transistors M8 and M9 used in the output stage of the circuit.

The implementation of M1 makes possible to realize controlled power delivery path to the circuit. As compared with the conventional scheme, where the power delivery path is made up of direct connection of the switching network to the supply voltage, the new power-gating structure realizes regulation of the current provided to the circuit. This feature is necessary for improvement of the operating efficiency and stable operation of the circuit during switching and transient disturbances.

The use of M5 in the proposed circuitry is considered to be the main modification of the circuit. This transistor is added to the regenerative feedback network of the circuit in order to enhance the feedback circuit responsible for the generation of the hysteresis. Due to this, the difference between the upper and lower switching threshold of the circuit is increased providing more wide hysteresis window than that of the conventional Dual-Mode Schmitt Trigger. Thus, the noise

immunity of the circuit is increased as well as the switching of the circuit is not produced under action of slowly varying input signals.

In order to enhance the output behavior, M8 and M9 transistors are added to the output stage of the circuit. They increase the stability of the output stage and help to produce the reliable switching in transient mode and better transient recovery in case of Single Event Transient (SET) analysis.

As a result of the structural changes performed, the performance of the circuit is significantly improved. First of all, due to adaptive feedback circuit, the width of hysteresis is increased from 194.63 mV in the conventional Dual-Mode Schmitt Trigger to 317.76 mV in the proposed circuit. Also, the power-gating structure and enhanced output stage of the circuit make possible stable transient recovery during SET current injection analysis. In spite of additional transistors needed for the implementation of the circuit, the hardware complexity is decreased by improvements in switching reliability and noise immunity of the circuit.

Thus, the proposed adaptive hysteresis Dual-Mode Schmitt Trigger retains the main advantages of the conventional DST circuitry and eliminates its disadvantages.

IV. SIMULATION METHODOLOGY

In the proposed Dual-Mode Schmitt Trigger circuit, the design and simulation were performed using the Cadence Virtuoso Analog Design Environment (ADE) with the 90 nm CMOS technology. The purpose of performing the simulations was to study the switching characteristics, hysteresis behavior, power dissipation, propagation delay, and transient robustness of the proposed Dual-Mode Schmitt Trigger circuit. The same simulation conditions were applied to both the conventional and proposed Dual-Mode Schmitt Trigger circuits in order to compare their performances.

The size of transistors was chosen according to the design criteria in order to obtain a stable switching characteristic with the minimal power dissipation. The simulations have been carried out using the supply

voltage of 1.2 V at 27°C operating temperature and typical process conditions. Both the conventional and proposed Dual-Mode Schmitt Trigger circuits were simulated under the same conditions, in order to compare their performances.

The hysteresis properties of the circuits were investigated by means of the DC sweep analysis, when the input voltage is varied and the upper and lower threshold voltages of the circuit are determined to calculate the hysteresis width as the difference between the two threshold voltages. Dynamic switching characteristic has been studied using the transient analysis when time dependent signals are applied to the circuit. With such type of simulation one can investigate the output signal and switching behavior as well as propagation delay of the circuit.

The ability of the proposed circuit to withstand the radiation induced disturbances has been investigated through the Single Event Transient (SET) analysis, which included injecting the transient current pulses into the sensitive circuit node. The recovery behavior of the proposed circuit was compared with the recovery behavior of the conventional Dual-Mode Schmitt Trigger circuit in order to assess the improvement of transient tolerance.

The power consumption was calculated during the operation of the circuit using Cadence power analysis tool, while propagation delay was calculated from the transient analysis data, as the difference in time between the switching points of the input and output signals. The performance of the proposed circuit was assessed through the comparison of simulation results of both the conventional and proposed Dual-Mode Schmitt Trigger circuits.

V. RESULTS AND DISCUSSION

Performance analysis of the proposed Adaptive Hysteresis Dual-Mode Schmitt Trigger is carried out using Cadence Virtuoso Analog Design Environment (ADE) with 90nm CMOS technology. The performance of the circuit was analysed under similar simulation conditions to assess its functionality, DC transfer behavior, transient behavior, and SET resistance capability. The results obtained from simulations prove that the proposed adaptive hysteresis mechanism works effectively.

A. FUNCTIONAL VERIFICATION

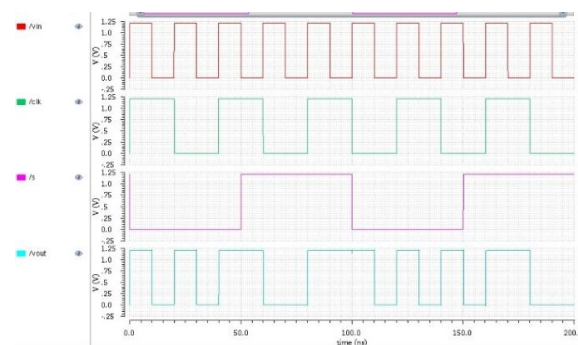


Fig 3: Functional Simulation of the Proposed Dual-Mode Schmitt Trigger

Functional correctness of the proposed adaptive hysteresis Dual-Mode Schmitt Trigger was confirmed using Cadence Virtuoso transient simulation. Figure 3 represents the dependence of the input signal (V_{in}), clock signal (CLK), control signal (CTRL), and output signal (V_{out}).

It can be seen from the provided simulation that the circuit operates properly depending on various input and control conditions. Output signal follows the required switching pattern depending on the applied input and control signals, and logic levels remain stable during the entire simulation process. Generated output waveform is synchronized properly with the clock signal. Therefore, the functional verification proves that the proposed circuit works properly performing the intended operation and thus forming the basis for electrical performance evaluation.

B. DC TRANSFER CHARACTERISTICS

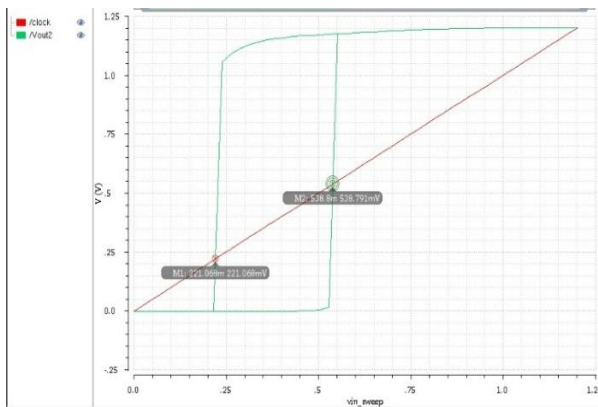


Fig 4: DC Transfer Characteristics of the Proposed Dual-Mode Schmitt Trigger

The DC transfer characteristics for the adaptive hysteresis Dual-Mode Schmitt Trigger were acquired through DC sweep analysis in Cadence Virtuoso. DC sweep was performed from 0 V to 1.2 V and then sweeping back to get the voltage transfer characteristics of the circuit. This results in hysteresis characteristics, illustrated in Figure 4. Upper and lower switching threshold voltages were extracted from the forward and reverse transfer curves respectively. The hysteresis width of the circuit is defined as the difference between the switching threshold voltages. It was observed that the circuit designed here provides a hysteresis width of 317.76 mV through simulations.

The adaptive feedback system included in this design has made the switching process more regenerative and increased the difference between the switching thresholds. Therefore, the designed circuit has wider hysteresis window, which makes the circuit more immune to the noise signals and minimizes false switching for slowly varying input voltage values.

C. TRANSIENT ANALYSIS

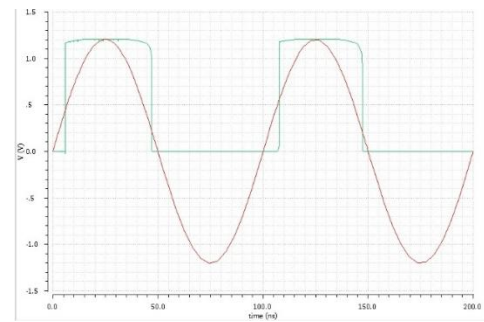


Fig 5: Transient Response of the Proposed Dual-Mode Schmitt Trigger

The transient analysis was carried out to determine the dynamics of the switching operation of the suggested adaptive hysteresis Dual-Mode Schmitt Trigger under time varying input conditions. Sinusoidal input voltage was used on the suggested circuit to obtain the output response, which is presented in Figure 5.

From the simulation, it is clear that there is correct switching of the output state either to logic high or logic low whenever the input voltage passes through the switching thresholds. The effect of hysteresis makes the switching of the output not to occur unnecessarily, making the output very stable even if the input voltage varies gradually. The transient analysis indicates that the suggested circuit operates reliably for switching purposes.

D. SINGLE EVENT TRANSIENT ANALYSIS

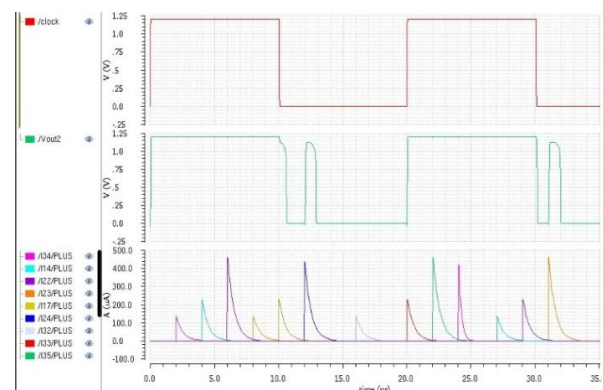


Fig 6: Single Event Transient (SET) Response of the Proposed Dual-Mode Schmitt Trigger

Resistance of the designed circuit against the radiation-induced disturbances was carried out by analyzing the Single Event Transients (SET). Here, a transient current pulse is applied to a sensitive node of the circuit in order to represent the impact of a particle hit, and then responses of the nodes of the circuit are observed.

As can be seen from Figure 6, a transient pulse generates some disturbances of voltages inside the circuit. Nevertheless, adaptive hysteresis approach can suppress these disturbances, thus returning the output to its normal working state. In other words, regenerative feedback circuitry and optimized output stage play their role in recovering the system after transient disturbance. Thus, according to the SET analysis, it has been proved that adaptive hysteresis Dual Mode Schmitt Trigger has improved resistance to transients.

E. PERFORMANCE COMPARISON

Table I. Performance Comparison between Existing and Proposed Dual-Mode Schmitt Trigger

Parameter	Conventional DST	Proposed DST
Power Consumption (μW)	6.52	9.74
Propagation Delay (ps)	114.92	112.04
Hysteresis Width (mV)	194.63	317.76
Area (μm^2)	0.545	1.48
PDP (aJ)	749.66	1091.28
EDP (zJs)	86.14	122.27

Table I below compares the performance of the traditional and the proposed Adaptive Hysteresis Dual-Mode Schmitt Trigger Circuits at identical simulation conditions. The comparison involves power dissipation, propagation delay, hysteresis voltage width, silicon area, Power Delay Product (PDP) and Energy Delay Product (EDP).

Hysteresis width of 317.76 mV is attained using the proposed circuit whereas the traditional hysteresis width is 194.63 mV, giving an increase of about 63.3%. Increased hysteresis improves noise tolerance of the circuit and stability of switching by minimizing the output transitions caused by slowly changing and noisy input signal.

Propagation delay is improved from 114.92 ps to 112.04 ps. This shows that addition of adaptive feedback circuit does not reduce switching speed. Instead, it leads to minor improvement in response time. Average power dissipation rises from 6.52 μW in the traditional to 9.74 μW in the proposed circuit. Likewise, silicon area increases from 0.545 μm^2 to 1.48 μm^2 owing to inclusion of additional transistor needed for adaptive feedback, power gating and output stage improvement.

Power Delay Product (PDP) is raised from 749.66 aJ to 1091.28 aJ whereas Energy Delay Product (EDP) is increased from 86.14 zJ.s to 122.27 zJ.s. This reflects the extra energy consumed by the enhanced circuitry. However, this trade-off is justified since considerable improvements in hysteresis, switching stability and transient robustness have been realized through the design of the new circuit.

Simulation results have clearly shown that the proposed Adaptive Hysteresis Dual-Mode Schmitt Trigger Circuit offers better switching characteristics than the traditional one. Though the enhanced circuitry consumes more power and uses additional silicon area, the improvement in hysteresis characteristics and transient robustness makes it an appropriate candidate for applications involving reliable CMOS switching circuits.

VI. CONCLUSION

This paper described the design and implementation of Adaptive Hysteresis Dual-Mode Schmitt Trigger using 90 nm CMOS technology. The proposed circuit improves on the conventional Dual-Mode Schmitt Trigger circuit by introducing a power-gating transistor, an adaptive feedback transistor, and an improved output stage. These modifications in the architecture have significantly improved the regenerative switching mechanism, leading to an increase in hysteresis width, stability, and transient robustness of the circuit. The circuit has been designed and simulated using the Cadence Virtuoso Analog Design Environment (ADE). Its performance was then verified through functional verification, DC Sweep Analysis, Transient analysis, and Single Event Transient (SET) analysis.

The results of the simulation show that the circuit has a hysteresis width of 317.76mV compared to 194.63mV of the conventional circuit, which amounts to an improvement of

about 63.3%. Moreover, the proposed circuit has a reduced propagation delay of 112.04ps. Even though the proposed architecture consumes more power and requires additional silicon area, these drawbacks are compensated for by the substantial improvements in stability and robustness to transient and noise. Hence, the proposed Adaptive Hysteresis Dual-Mode Schmitt Trigger can be implemented successfully in applications where reliable and robust CMOS Switching Circuits are required.

VII. FUTURE SCOPE

The above mentioned adaptive hysteresis Dual Mode Schmitt Trigger forms the basis for future development in designing highly reliable low power CMOS circuits. Future research may involve fine tuning of transistor sizing and adaptive feedback network in order to achieve lower power dissipation and smaller silicon area requirements without sacrificing the benefits of increased hysteresis levels. Other optimization methodologies can be considered in order to decrease PDP and EDP without compromising on the switching reliability.

The proposed approach can be realized using advanced CMOS technology nodes such as 65 nm, 45 nm and FinFET technologies in order to test the scalability and performance of the proposed design under modern manufacturing techniques. Moreover, extensive simulations in different process voltage temperature (PVT) and radiation conditions can be performed in order to test the reliability of the proposed circuit. Future studies may include investigation of the use of this adaptive hysteresis circuit in designing high speed digital interfaces and sensor front-end analog circuits.

REFERENCES

- 1) "Radiation Hardened Domino Logic-based Schmitt Trigger Circuit With Improved Noise immunity," *IEEE Trans. Device Mater Rel.*, VOL. 24, NO. 4, Dec. 2024.
- 2) A.P.Shah, N.Yadav,A.Beohar,and S.K.Vishvakarma, "Process variation and NBTI resilient Schmitt trigger for stable and reliable circuits,"*IEEE Trans. Device Mater.rel.*, vol.18,no.4,pp.546-556,Dec.2018.

- 3) N.Singh, S.Shekhar and A.Angeline, "Schmitt trigger designs using domino logic style," *ECS Trans.*,vol.107,no. 1,p.8885,2022.
- 4) S. B. Ramakrishna, S. Madhusudhan, B. Nikshep, B. Naveen, and H. D. Teertha prasad, "Power and delay optimization of domino Schmitt trigger configurations with enhanced hysteresis voltage," *Analog Integer. Circuits Signal Process.*. vol.102,no.1,pp.53-61,2020.
- 5) M. J. Gadlage, J. R. Ahlbin, P. gadfort, A. H. Roach, and S. Stansberry, "Characterization of single-event transients in Schmitt trigger inverter chains operating at subthreshold voltages," *IEEE Trans.Nucl. Sci.*,[6] vol.64, no. 1,pp. 637-642, Jan.2017.
- 6) S. Al-Sarawi, "Low power Schmitt trigger circuit," *Electron. Lett.*, vol. 38, no. 18, p. 1, 2002.
- 7) A. Panda,A. K. Singh, R. Tirupathi, and S. K. Kar, "A low-power tuable square-wave generator for instrumentation applications," *IEEE [8] Trans. Instrum. Meas.*, vol.69, no.7, pp. 5051-5057, Jul. 2020.
- 8) T. D. Fernandes, C. Galup-Montoro, and M.C. Schneider, "Analysis and design of the three-invertet Schmitt trigger for supply voltages down to 50 mV," *IEEE Trans. Circuits Syst. II,Exp. Briefs*, vol. 68, no. 7, pp. 2302-2306, Jul. 2021
- 9) K. Kim and S. Kim, "Design of Schmitt trigger logic gates using DTMOS for enhanced electromagnetic immunity of subthreshold circuits," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 5, pp. 963–972, Oct. 2015.
- 10) L. A. P. Melek, A. L. da Silva, M. C. Schneider, and C. Galup- Montoro, "Analysis and design of the classical CMOS Schmitt trigger in subthreshold operation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 869–878, Apr. 2017.
- 11) S. Dasgupta and R. Kar, "Single Event Transient Analysis of Schmitt Trigger Inverter Chains Using Current Injection Technique," *Microelectronics Reliability*, 2024.
- 12) S. Dasgupta and R. Kar, "Domino Logic Based Schmitt Trigger Circuit for Low-Power VLSI Systems," *Microelectronics Reliability*, 2024.

