

DESIGN AND IMPLEMENTATION OF REVERSIBLE VEDIC MULTIPLIER WITH USING BVF, BME GATE, CNOT GATE, AND PERES GATE

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Abstract: The Vedic mathematical algorithm has been developed by ancient Indian and there have been 16 sutras available. Urdhva Tiryakbhayam (UT) is one of the Vedic mathematic algorithm that can be applied to all cases of multiplications viz. Binary, Hex, and also Decimals. It is based on the concept that the generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in the generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers, with the increase in the number of bits of multiplicand and/or multiplier, the time delay in the computation of the product does not increase proportionately. Because of this fact, the time of computation is independent of the clock frequency of the processor. In this phase, the Vedic multiplier (VM) has been designed and implemented using a reversible gate. The main object of the work is to design an efficient multiplier which aims at lowering the value of proposal restriction. The fast, low-power reversible logic and VM with lower hardware density have combined and have brought about in a lessening in TRLIC of the anticipated design equated to the other designs.

Keywords: Reversible gate, Vedic multiplier, BVF, BME, PERES, CNOT, Garbage Outputs, Constant inputs, Gate Counts, Quantum cost

I. INTRODUCTION

Reversible is an auspicious processing plan worldview that gives a strategy for

developing PCs no heat scattering. Reversible process stands up because of the operation of quantum mechanics values in the direction of the improvement of an all-inclusive figuring machine. In specific, the essentials of reversible processing rest on the construction among entropy, heat move between atoms in a framework, the likelihood of a quantum molecule concerning a detailed state at some random time, and the quantum electrodynamics between electrons when they are in portion nearness.

The fundamental guideline of reversible process is that a objective gadget with a hazy number of data and yield lines will create figuring climate where the electrodynamics of the framework takes into account the forecast of all future states dependent on identified past states, and the framework arrives at each possible state, transporting about no warmth scattering.

A reversible rationale door is a N-input N-yield rationale gadget that gives balanced planning between the information and the yield. It not just encourages us to decide the yields from the sources of information, yet additionally causes us to exceptionally recuperate the contributions from the yields. Trash yields are those which don't add to the reversible rationale acknowledgment of the plan. QC alludes to the expense of the circuit regarding the expense of a crude entryway. Door tally is the quantity of reversible entryways used to understand the capacity. Entryway level alludes to the quantity of levels which are needed to understand the given rationale capacities.

II. REVERSIBLE GATES

A reversible logic gate is a gate that maps a unique set of input states to a unique set of output states (a one-to-one or bijective mapping). Unlike traditional logic gates (such as AND or OR), reversible gates uniquely reconstruct the original inputs directly from the outputs. The following are the important design constraints for reversible logic (RL) circuits.

1. RL gates do not allow fan-outs.
2. RL circuits should have minimum quantum cost.
3. The design can be optimized to produce the minimum number of garbage outputs
4. The RL circuits essential use the minimum number of constant inputs.
5. The RL circuits essential use a minimum logic depth or gate levels.

A. BVF gate

BVF gate is the 4×4 gate with 4 input and output with the QC of 2. The fig. 1 represents the input and output vector of the BVF gate.

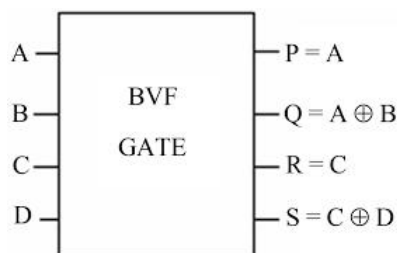


Fig. 1. Block Diagram of BVF gate

B. BME gate

BME gate is the 4×4 gate with 4 input and output with the QC of 5. The fig. 2 represents the input and output vector of the BME gate.

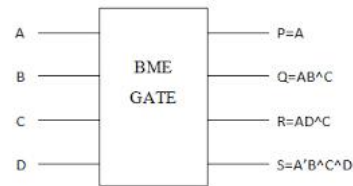


Fig. 2. Block Diagram of BME gate

C. PERES gate

PERES gate is the 3×3 gate with 3 input and output with the QC of 4. The fig. 3 represents the input and output vector of the PERES gate.

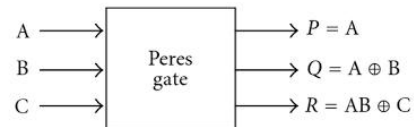


Fig. 3. Block Diagram of PERES gate

D. Feynman gate

The controlled not gate (CNOT) has been represented as Feynman gate. It has two input and output with the QC of 1. It is the 2×2 gate has been used for fan-out process. The fig. 4 represents the input and output vector.

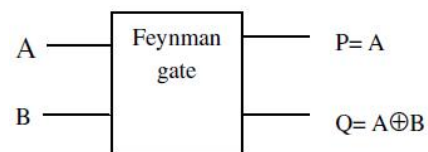


Fig. 4. Block Diagram of Feynman gate

III. DESIGN AND IMPLEMENTATION OF URM USING BVF GATE, BME GATE, PERES GATE AND CNOT GATES

In this work, the circuit has been considered using one BVF, two BME, one PERES, and one CNOT reversible gate. The limited products have been generated using BME reversible gates. The CNOT gate has been used to perform the operations of copying the output and perform the EX-OR operations. This phase design requires three

Constant input (CI) and four reversible gates have been used with the quantum cost (QC) and it has been generated six garbage output (GO). TRLIC of this anticipated circuit is 27, which is comparably lesser than the prevailing circuit.

The Fig. 5 shows the block diagram of the proposed circuit design with 1 BVF, 2 BME, 1 PERES, and 1 CNOT gate. The BVF obtained the input $(b_0, 0, b_1, 0)$ and produces the 4 output (b_0, I_0, b_1, I_1) . The first BME gate with the 4 input $(a_0, b_0, 0, b_1)$ and 4 output value, the first and fourth output has been the garbage (g), the second output has been considered the O_0 and third output has been one of the inputs for PERES gate it has been same for the second BME gate and second output has been input for the PERES gate and third output has been the input for the CNOT gate. In PERES gate 2, input has

been obtained from the BME gates and one constant input. The output of the PERES has been considered as out 1 and one garbage output. The remaining output has been connected to the input of the CNOT gate. The 2×2 CNOT gate gets one input from the second BME and one from the PERES gate. The two outputs have been connected to final out3 and out2. Finally, BVF, BME, PERES and CNOT gate produces one final output, O_0 has been obtained from the first BME gate, O_1 has been obtained from the PERES gate, The O_2 and O_3 has been obtained from the CNOT gate.

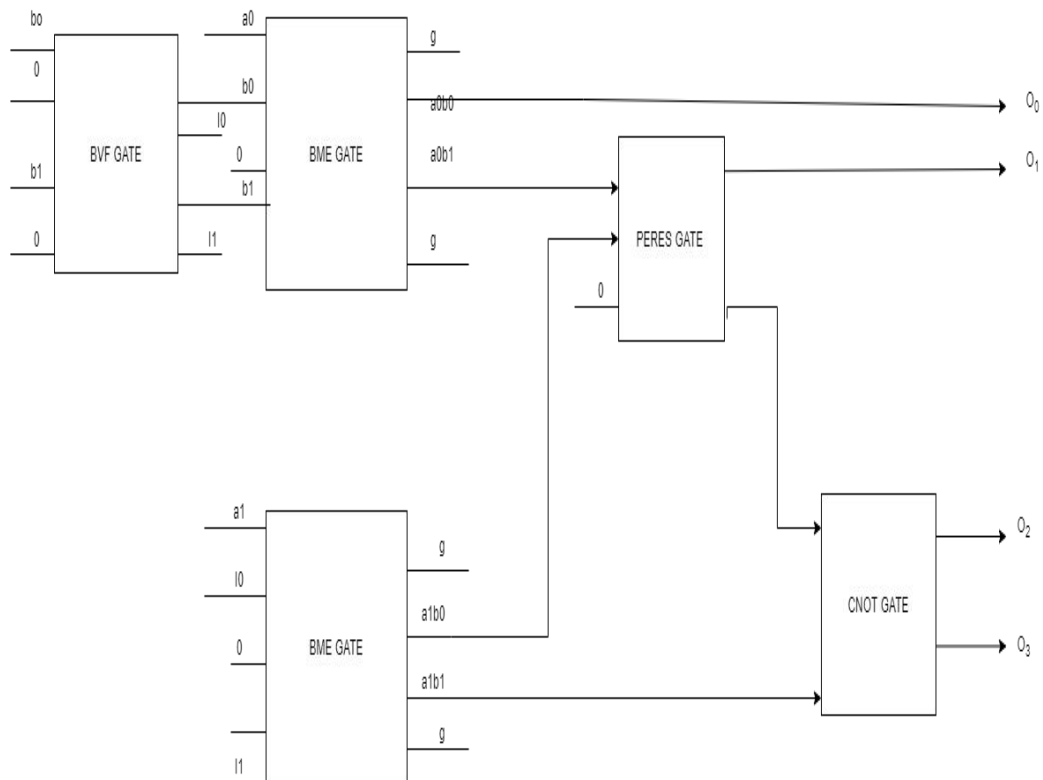


Fig. 5. Block Diagram of 2×2 reversible Vedic multiplier

A. Implementation of 2×2 reversible Vedic multiplier

A 2×2 UTM using RLG of BVF, BME, PERES, and CNOT gate implemented on reversible expressions. In manipulative the 2×2 UT Multiplier using reversible logic is as shown in the fig. 5. The partial product has been generated by 4 reversible gates and 4 outputs have been measured with the quantum cost of 15.

The synthesis result shown in the Fig.6 represents the reversible gates designed with constant input a and b. A BVF accepts 4-input and produces 4-output.

Each BME gate accepts 4-input bits; 2-bits from multiplicand and the other 2-bits from the multiplier. The PERES gate accepts 3 inputs, two inputs from the BME gate, and one constant input value. The CNOT gate accepts the 2 input, one is from PERES gate and one is from second BME. The final output has been reduced; the main intention of this approach is to diminish the output by garbage output.

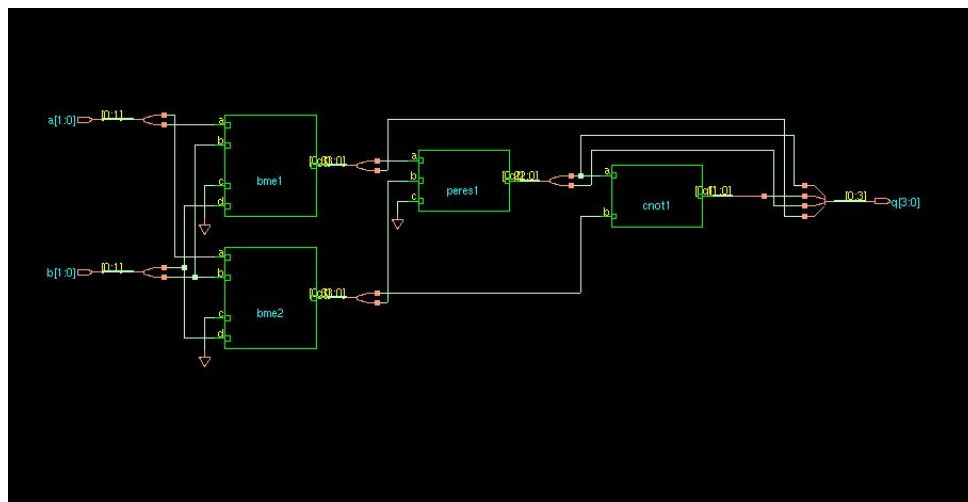


Fig. 6. Synthesis result of 2×2 reversible Vedic multiplier

IV. RESULT AND ANALYSIS

In this phase, the Vedic multiplier has been designed and implemented using a reversible gate, the main object of the work is to design an efficient multiplier aims at lowering the value of proposal restriction. The fast, low-power reversible logic and VM with lower hardware density have combined and have bring about in a lessening in TRLIC of the anticipated design equated to the other designs.

TRLIC is calculated based on the equation (1),

$$\text{TRLIC} = \Sigma (\text{NG}, \text{QC}, \text{CI}, \text{GO}) \dots (1)$$

Where TRLIC has been represented as total reversible logic implementation cost, where NG is number of gates, QO is Garbage Outputs, CI represents Constant inputs, Gate QC represents Quantum cost.

In-circuit design, there have been two main concerns about the optimization they are area and delay. There has been plenty of research that has been carried out to the circuit level to study the trade-offs among them. In specific, transistor sizing has been well recognized as a good way to

reach decreases in the delay of circuits, while the ensuing increase in rectangular area from transistor sizing can be minimized by special circuit design called reversible logic.

Another most important performance metric is power. As wireless communication and mobility of gear developed gradually required, the power dissipation of circuits has become a key alarm in circuit synthesis. In a performance-driven synthesis of VLSI circuits, the low-power design has merged the grades of area and delay as major inspirations in optimization. The circuit design, there is a need to confirm low power dissipation while sustaining delay limits. In this phase, the reversible logic gate and Vedic mathematics have been used to minimize the area, delay as well as power consumption.

In table I, the performance metrics of TRLIC has been measured as 32 with the results of Garbage Outputs of 5, Constant inputs (CI) of 5 of Gate Counts (GC) of 5, Quantum cost (QC) 17. Table II describes the comparison TRLIC value of 4x4, 8x8, 16x16 and 32x32. The figure 7 evaluate implementation results of various bits.

In table III, the performance metrics of Area, power and delay comparison of various bits with proposed model. The table IV describes the TRLIC of proposed work has been compared with the two-existing model with the results of Garbage Outputs of 5, Constant inputs (CI) of 5 of Gate Counts (GC) of 5, Quantum cost (QC) of 17.

TABLE I. COMPARISON OF 2X2 REVERSIBLE VEDIC MULTIPLIER

Measurement	Method 1
Garbage Outputs	5
Constant inputs (CI)	5
Gate Counts (GC)	5
Quantum cost (QC)	17
TRLIC	32

TABLE II. COMPARISON OF 4X4, 8X8, 16X16 AND 32X32 REVERSIBLE VEDIC MULTIPLIER

TRLIC	METHOD 1
4X4	303
8X8	1555
16X16	6899
32X32	28947

TABLE III. COMPARISON OF AREA, POWER AND DELAY

Parameters	Area(Gate Count)	Power(mW)	Delay(ns)
2x2	24	81.0	7.809
4x4	204	116.30	17.490
8x8	1026	190.47	33.019
16x16	4578	352.84	53.559
32x32	19260	693.84	96.512

TABLE IV. COMPARISON RESULT OF TRLIC PARAMETER WITH EXISTING METHODS

Measurement	Proposed method1	EM1	EM2
Garbage Outputs	5	9	5
Constant inputs (CI)	5	4	5
Gate Counts (GC),	5	6	5
Quantum cost (QC),	17	21	23
TRLIC	32	40	38

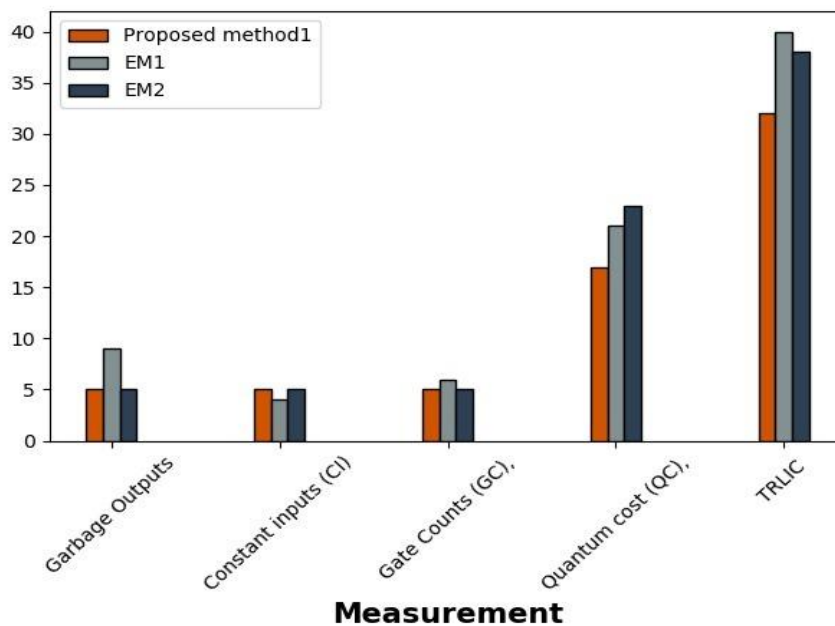


Fig. 7 Implementation results of existing models

V CONCLUSION

Vedic Multiplier is one of the best solutions which are capable of performing the quicker multiplications by eliminating the unwanted steps in the multiplication process. In this work, the reversible Vedic multiplier with the reversible logic gates of BVF, BME, PERES and CNOT has been implemented in Vedic multipliers of various sizes has been simulated. The performance metrics of power, delay, and the area has been measured with the synthesis result and simulation result. The simulation results, observed for all the variations of bits and performance metrics of various prevailing and anticipated method. The result shows that the proposed work obtains the Garbage Outputs of 5, Constant inputs (CI) of 5 of Gate Counts (GC) of 5, Quantum cost (QC) of 17 and TRILC value of 32.

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